GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Contract No. F29601-87-C-0202

Semiannual Technical Report for September, 1990 through April, 1991

August 8, 1991

PROGRAM MANAGER
Dr. Robert C. Vehse
AT&T Bell Laboratories
Reading, Pennsylvania
Office: (215) 939-6277
FAX:(215) 939-3175

ADMINISTRATIVE CONTACT
Mr. E. F. Lapham
AT&T Federal Systems Division
Greensboro, North Carolina
Office: (919) 279-3202
FAX:(919) 279-5381

Prepared for
DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
DARPA/DSO
1400 Wilson Boulevard
Arlington, VA 22209-2308

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GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Semiannual Technical Report
April, 1991

1. INTRODUCTION (S. F. Nygren)

The Gallium Arsenide Pilot Line for High Performance Components (Pilot Line III) is to develop a facility for the fabrication of GaAs logic and memory chips. We have completed the first forty-eight months of this contract, and this report covers the period from September 24, 1990, to March 24, 1991. In addition, an appendix provides a final report for the Advanced Technology we developed to provide 400 MHz circuit operation (twice as fast as the requirement for the baseline technology).

Wafer fab starts remained suspended for the first four months of this six-month reporting period. The suspension began in June, 1990, when we lost control of the EFET threshold voltage and determined that control could not be regained unless we made a fundamental change to the process for etching EFET tubs. To conserve resources, we stopped almost all program work except for development and verification of a new etching technology.

Physical and electrical analysis conclusively demonstrated that the EFET problem was caused by residual AlGaAs remaining in the EFET tubs. For our Self-Aligned Refractory Gate Integrated Circuit (SARGIC) process to perform as designed, the FET gates must be placed directly on GaAs. Residual AlGaAs increases the FET thresholds and thereby substantially changes device characteristics. We solved the problem by developing a new etch process using a "PP" etchant (H_3PO_4 and H_2O_2). AlGaAs is now completedly removed from EFET tubs and EFET threshold control has been restored. As a bonus, the new process also solves the EFET scaling problem; large and small EFETs now have the same thresholds and currents per unit width. Wafer fab resumed in February, 1991, and there were a few completions before the end of March. We shall start testing primary circuits from these wafers in April.

With wafer starts suspended and other program work minimized to conserve resources, there was little primary circuit testing. A new result is that the 32-Bit Multiplier is functional at 60 MHz. It has 77 gates in its critical path. Also, the Cell Array Casino Test Chip was demonstrated up to 83 MHz (18 gates in its critical path). To conclude the program, we are preparing 16 final lots: eight 4K SRAM II, four 32-Bit Multipliers, and four Cell Array Casino Test Chip. These will be the first wafers to have EFETs and DFETs on target and to also have no scaling problems. That is, we expect the FETs to match the circuit design model.

In our reliability studies, we completed the first of two rounds of High Temperature Operating Bias (HTOB) reliability experiments with the PT-2M memory. This memory is known to have lower resistance to bit flipping than the redesigned 4K SRAM. Nevertheless, it has reliability similar to other GaAs circuits: the maximum failure rate at 65°C over ten years is 75 FITs at ten years.

2. DEMONSTRATION VEHICLES

2.1 Circuit Overview (C. H. Tzinis, S. F. Nygren)

This contract requires SRAM, Custom Logic, Standard Cell Logic, and Cell Array Logic circuits that operate at a 200 MHz clock over -55 to 125°C. To achieve this goal, we designed five sets of small scale circuits (PT-0, PT-1, PT-2L, PT-2M, and 1K Cell Array) plus eight full size circuits, as shown in Table 1.

TABLE 1 — Circuits Designed for Pilot Line III

	Style	Size	Status
PT-0	Custom	FETs Only	Work Complete
PT-1	Various	Small Logic	Work Complete
	Various	Unclocked 256-bit SRAM	Work Complete
PT-2L	Various	364-2211 Logic Gates	Work Complete
PT-2M	Various	91-283 Logic Gates	Work Complete
	Custom	Clocked 256-bit SRAM	Work Complete
1K Cell Array	Cell Array	738 Logic Gates	Work Complete
4K SRAM	Custom	4096-bit SRAM	Work Complete
4K SRAM II	Custom	4096-bit SRAM	In Testing
32-Bit Multiplier	Custom	6500 Logic Gates	In Testing
ALU	Custom	3571 Logic Gates	Work Complete
ALU	Std. Cell	3452 Logic Gates	Work Complete
Transversal Filter	Std. Cell	5190 Logic Gates	Work Complete
Casino Test Chip	Std. Cell	3700 Logic Gates	Work Complete
Casino Test Chip	Cell Array	4126 Logic Gates	In Testing

A rigorous evaluation of each circuit would consider five criteria:

Functionality	Logic: pass all test vectors at 25°C Memory: all bits work at 25°C
V_{DD}	Works for $1.8 < V_{DD} < 2.2V$
I/O	Complies with all I/O voltage specifications $V_{IH} \leq 0.9$, $V_{IL} \geq 0.3$, $V_{OH} \geq 1.0$, $V_{OL} \leq 0.2V$
Speed	Logic: works at 200 MHz for 15-20 gate delays Memory: works at 200 MHz
Temperature	Works from -55 to 125°C

We now have test results for all circuits except the second iteration of the 4K SRAM (4K SRAM II). The best results for the full-sized circuits are given in Table 2. For some circuits, more than one example is given.

TABLE 2 — Best Circuit Results

Memory

• PT-2M	— Satisfies functionality, V_{DD}, I/O, and speed for 0-80°C — Satisfies functionality, I/O, and temperature at 50 MHz over part of the V_{DD} range.
• 4K SRAM I	— Satisfies functionality, V_{DD}, and I/O at 40°C and 50 MHz.
• 4K SRAM II	— No test data, yet.

Custom

• ALU	— Satisfies functionality, speed, and temperature at V_{DD} = 2.0V, but fails one of the four I/O specifications. — Satisfies functionality, V_{DD}, and speed over 25-125°C, but fails one of four I/O specifications.
• 32-Bit Multiplier	— Passes all 4096 test vectors at room temperature — Operates up to at least 60 MHz between 0°C and 55°C — Note: Test results are incomplete

Standard Cell

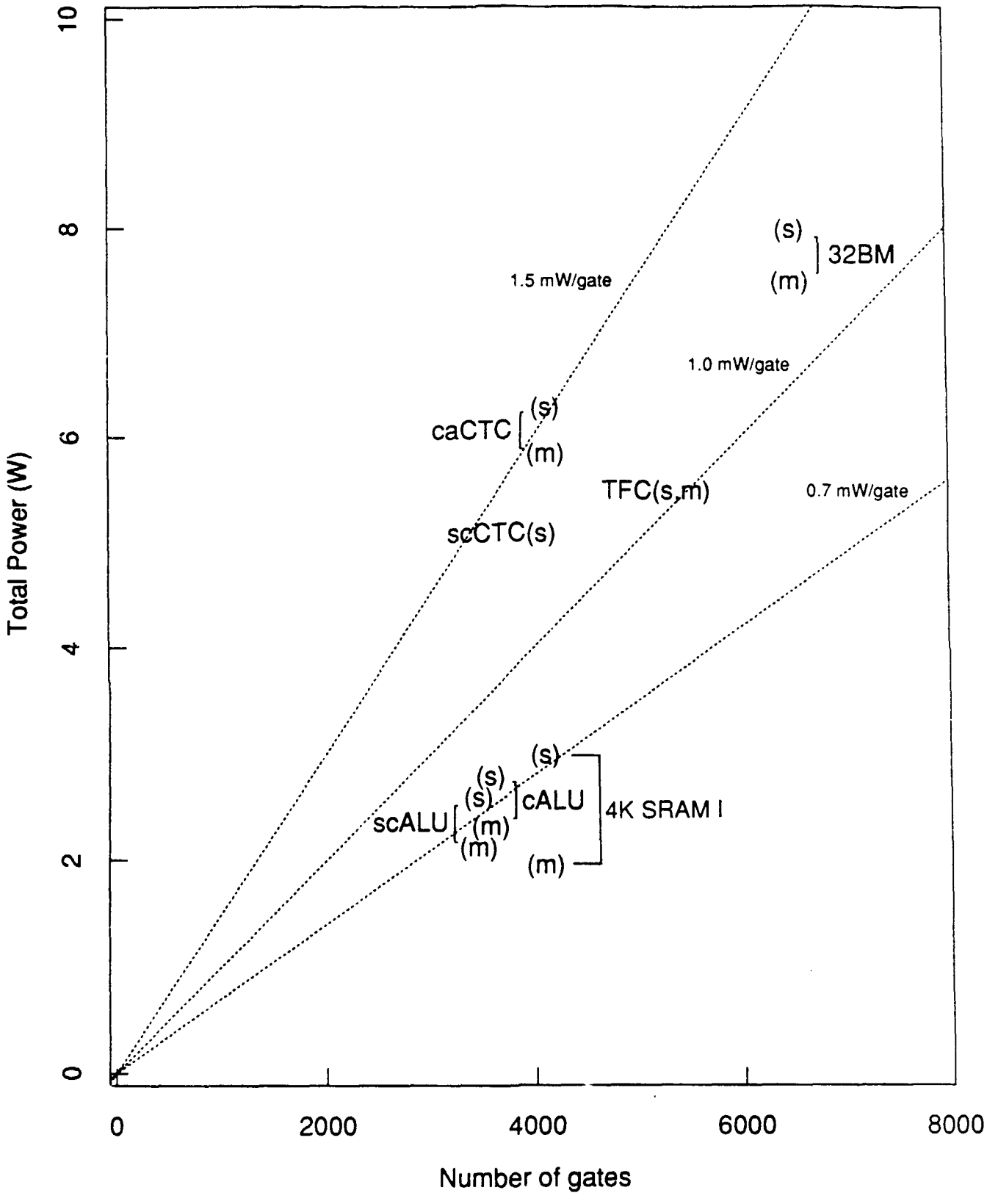
• ALU	— Satisfies functionality, V_{DD}, and I/O at 125 MHz and 25°C
• Transversal Filter	— Satisfies functionality, V_{DD}, and I/O at room temperature up to 40 MHz (the limit of the test equipment)

Cell Array

• 1K Cell Array	— Satisfies functionality, V_{DD}, and I/O at 100 MHz and 25°C — Satisfies functionality, speed, and temperature at 2.2V, but fails one of the four I/O specifications.
• Cell Array Casino Test Chip	— Satisfies functionality up to at least 80 MHz — Note: Test results are incomplete

Due to the suspension of wafer starts during much of this reporting period, there are only two new entries in this table. First, the 32-Bit Multiplier is functional, and it operates up to at least 60 MHz between 0 and 55°C. (Since this device has 77 gates in its critical path, this is equivalent to 230 MHz when there are 20 gates in the critical path.) Second, the Cell Array Casino Test Chip has shown operation up to 80 MHz. It has 18 gates in its critical path.

These circuits draw from 2 to 8 watts. Figure 1 shows both the simulated (s) and measured (m) powers for 7 of the full-size circuits. In each case, the simulation gives a good approximation of the actual power, with the measured power being slightly lower than simulation in all cases.



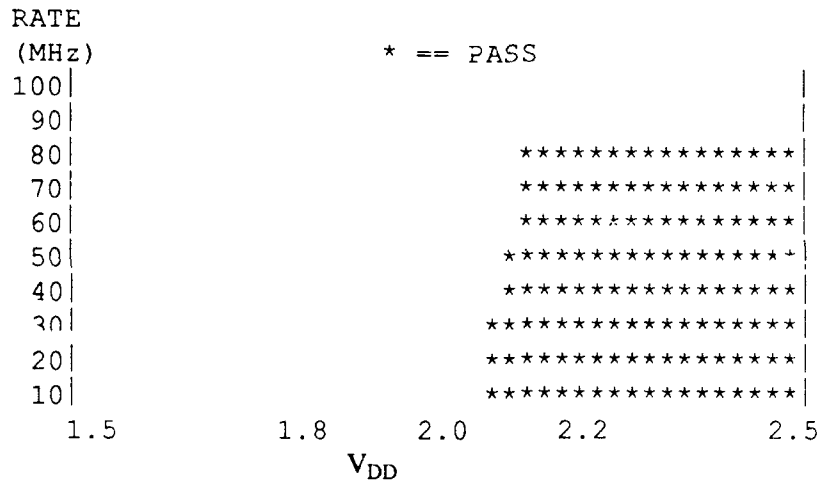
Measured and Simulated Power for Pilot Line Circuits

Figure 1.

2.2 Cell Array Casino Test Chip Test Results (J. Scorzelli)

In the previous Semiannual Report, we verified the Cell Array Casino Test Chip (CA-CTC) design by identifying a fully functional wafer die at 2.2V V_{DD} [Wafer number 36026, location (2,-2)]. At that time, DC and preliminary AC test data were collected and reported. We found the operating range was somewhat wider than the target 1.8 - 2.2V for V_{DD}, and the maximum speed was well over 40 MHz, which was initially thought to be the limit of the test fixture.

Currently, CA-CTC wafers are tested up to 100 MHz and packages will be tested up to 200 MHz. To date, the fastest chip, [wafer number 36133, location (2,-2)], runs at 83.33 MHz at 2.2V V_{DD} as determined by a linear speed search. (Packages are not yet available for testing at high frequency). A Speed vs. V_{DD} shmoo plot of this chip is shown in Figure 2. In the figure, the maximum passing region (denoted by asterisks), is at least 80 MHz. (The Y-axis resolution is 10 MHz).



Speed vs. V_{DD} Shmoo Plot

Figure 2.

We also measured four AC parameters: Data Propagation Delay, Data Setup Time, Data Hold Time, and Clocked Output Delay. All of the AC tests, with the exception of the Data Propagation Delay Test, require the counter section to be working, since the timing measurements are made with respect to the input clock edge, and the counter is the only synchronous section of the CA-CTC. The counter sections of seven wafer sites were functional at a V_{DD} of either 2.0V or 2.2V. Table 3 shows the measured timing data taken from these wafer sites. This table also shows the maximum operating frequency of each site.

TABLE 3 — CA-CTC AC Parametric Data

WAFER (LOC)	DATA PROPAGATION DELAY		DATA SETUP TIME		DATA HOLD TIME		CLOCKED OUTPUT DELAY		MAXIMUM OPERATING FREQUENCY
	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	@ V_{DD}
36133 (2,-1)	17ns	15ns	10ns	10ns	1ns	5ns	5.5ns	5.5ns	83.3MHz @ 2.2V
35571 (2,-1)	-	199ns	-	8ns	-	5ns	-	18.8ns	71.4MHz @ 2.5V
36026 (2,-2)	23ns	23ns	-	10ns	-	5ns	-	6.05ns	66.6MHz @ 2.5V
36133 (-1,-2)	251ns	18ns	-	12ns	-	22ns	-	6.9ns	66.6MHz @ 2.5V
36135 (1,-3)	14ns	16ns	-	-	177ns	-	5.5ns		47.6MHz @ 1.9V
35572 (1,0)	15ns	15ns	-	6ns	-	453ns	-	5.5ns	22.2MHz @ 2.3V
36135 (0,0)	-	-	220ns	216ns	479ns	479ns	42.5ns	83.8ns	*

Note that the fastest wafer site [wafer 36133, location (2,-1)], is also the most robust. That is, it operates at both 2.0V and 2.2V V_{DD} for all AC parameters. Also, the hold time measurement of 1ns at 2.0V for this site suggests an internal latching capability commensurate with very high speed operation.

The Propagation Delay measurement is made through the 32:1 Multiplexer section of the CA-CTC since it contains the critical path (worst-case delay). For this reason there is no direct relationship between the data propagation delay measurement and the other timing measurements. The V_{DD} level at which the Maximum Frequency is measured is determined by visual inspection of the Speed vs. V_{DD} shmoo plot. The dashes throughout the table indicate areas where no data transition was found. In the last line of Table 3, the asterisk in the Maximum Frequency column indicates the Speed vs. V_{DD} shmoo plot showed intermittent functionality and no V_{DD} voltage could be chosen in order to make a reliable linear search speed test.

2.3 32-Bit Multiplier (R. J. Niescier, L. R. Tate, L. Ackner)

In the previous Semiannual Technical Report, we described the initial test results for the 32-Bit Multiplier, in which we found chips with as few as 2 errors among the set of test vectors. The most promising of the initial lots was retested in November of 1990 with the cooperation of the multiplier design team. After correcting a small error in the design of the test vectors, we found a functional chip (wafer 36194) and several partially functional chips with as few as 2 errors. However, consistent behavior was difficult to obtain; the devices required one or two initialization vectors before correct operation would begin. To demonstrate the functional chip, each test vector was repeated 5 times, and the output was checked only for the fifth time. Using this procedure, the functionality of this site was demonstrated from 0 to 85°C.

Further tests at different temperatures revealed more repeatable behavior at the lower temperatures, and 60 MHz operation was obtained on the best functional site (two errors) at 0°C. The I/O level data at different temperatures were also obtained on this site, and the results are

shown in Table 4. This part matches simulations and satisfies the full I/O specification over the measured temperatures (25, 55°C). A linear extrapolation of these data suggests that this device would meet the I/O specifications over the entire military temperature range of -55 to 125°C. In comparison, the previous Semiannual Technical Report showed averages and ranges for a mixture of both devices with few errors and also partially functional devices that had marginal I/O buffers. This resulted in a large spread in I/O level data.

TABLE 4 — I/O Level Tests in Functional Part

Temperature	V_{OL}, mV range (average)	V_{OH}, mV range (average)	V_{IL}, mV range (average)	V_{IH}, mV range (average)
25°C	13-88 (60)	1200-1350 (1270)	404-552 (482)	414-550 (504)
55°C	28-97 (72)	1160-1320 (1230)	396-545 (465)	386-531 (482)
Target	<200	>1000	>300	<900

For many of the outputs, the CLOCK to DATA VALID delay was measured on an oscilloscope. The data showed a delay of 2 to 4 nS, which match expected simulation results.

We also tested a later lot that had been fabricated with the "PP" EFET tub etchant (see Section 3.3). We identified another functional device, but it required V_{DD} = 2.9V. This lot showed higher overall functionality than previous lots, but it also had the inconsistent operation and high number of shorts seen in the previous lot.

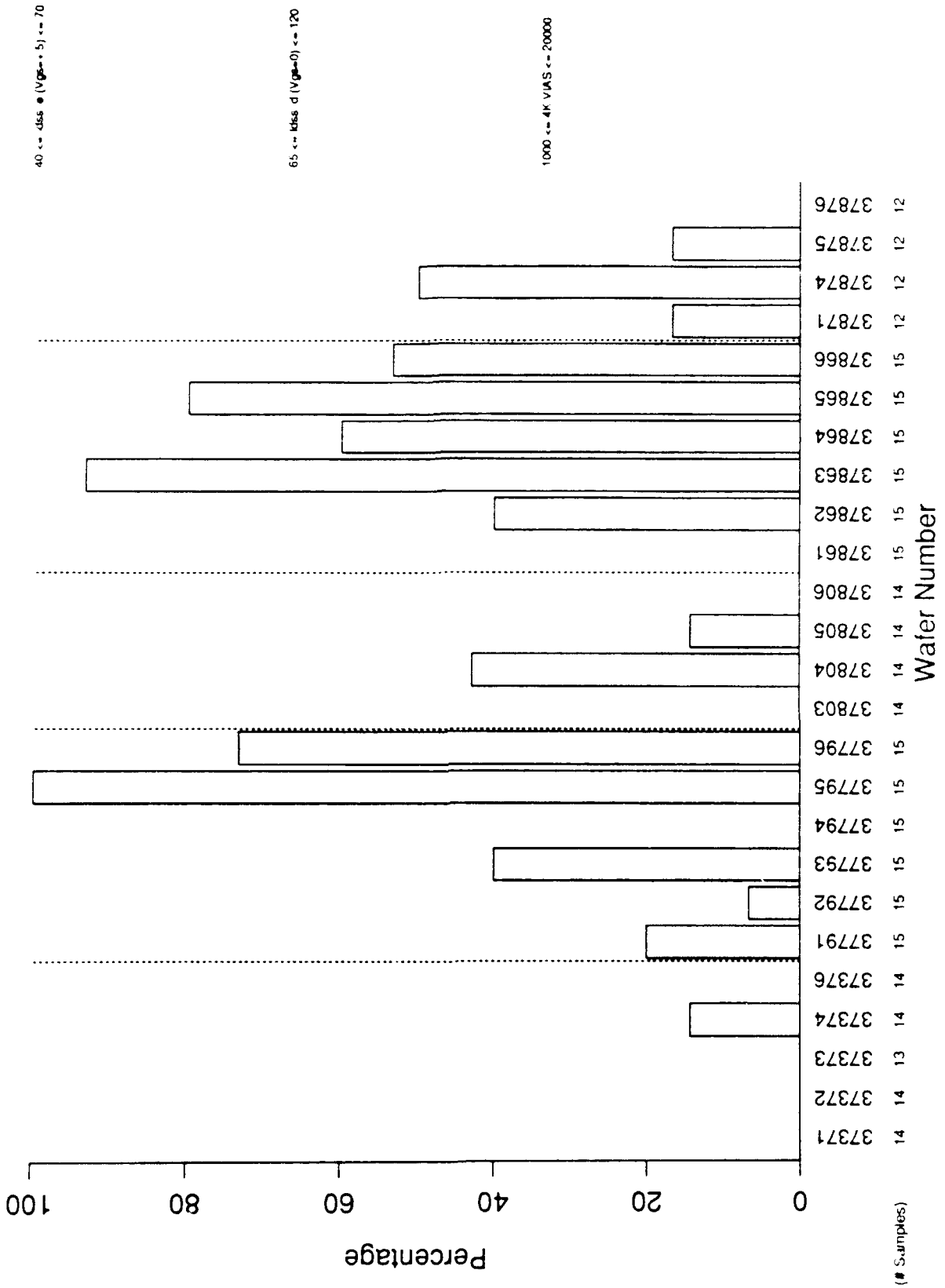
2.4 Yields and Learning Curves (C. H. Tzinis)

PCM Yield

Due to the resolution of the EFET threshold problem (see Section 3.3), the PCM yield for this period is substantially higher than for the previous period (40% good wafers vs. 17%). In the previous Semiannual Technical Report, we showed that primary circuit yield increases dramatically when more than 30% of a wafer's PCM sites are good, so we defined a "good" wafer as one having at least 38% good PCM sites. (The criteria are 40 < EFET current (V_{gs} = 0.5V) < 70 mA/mm, 65 < DFET current (V_{gs} = 0.0V) < 120, 1000 < 1.5 µm via chain resistance < 20,000 Ω). Figure 3 shows the PCM yield since the resumption of wafer fabrication. One wafer has a 100% PCM yield (wafer 37795).

D_0 Model for Shorts

The wealth of data available from our memory circuits allowed us to do Y_0/D_0 calculations for shorts (liftoff metallization technology) and interconnects (via technology). The memory circuits also allowed us to directly compare the same design in two different sizes, 256 bits and 4096 bits. The total "crossover" area between top and bottom metal was extracted electronically from the mask design information. Table 5 summarizes the percentage of shorts, top-to-bottom metal crossover area and calculated D_0 assuming Y_0 = 100% (no parametric failure allowed in short testing.)



PCM Wafer Yield (October, 1990 - March, 1991)

Figure 3.

TABLE 5 — Shorts in Memories

Code	Percentage Shorts (median)	Crossover Area (cm^2)	Crossover Area as a Percent of Chip Area	D_0 (cm^{-2})
PT-2M	2.85	1.8×10^{-3}	4.02	16.0
4K SRAM I	31.4	27.8×10^{-3}	9.88	14.0

The model used to calculate D_0 is

$$Y_D = Y_0 \left[\frac{1 - e^{-D_0 \cdot A_a}}{D_0 \cdot A_a} \right]^2$$

where A_a is the crossover area, and Y_D is the yield of the step (100% - 2.85% = 97.15% for PT-2M).

The derived D_0 is the defect density per crossover area and not per chip area. To get the contribution of shorts to the total defect density per unit chip area (D_0^T), we must multiply the D_0 for shorts times the crossover area as a fraction of chip area (e.g., 0.0988 x 14.0 cm^{-2} = 1.4cm^{-2}). Since D_0 from PT-2M (110 wafers) and D_0 from 4K SRAM I (34 wafers) are virtually the same, we believe the value is representative of our gold liftoff process.

Interconnect Yields

Our circuits contain large numbers of vias to connect one metal layer to another. For example, the 4K SRAM I has 223,805 vias, of which about half stand alone, and the other half are members of clusters that connect one bus to another. We can estimate circuit yield loss due to interconnects by constructing a model from via yields in our PCMs. Each PCM contains a via chain with 4300 1.5 µm vias connecting various metal layers in a repeating pattern. To model the yield due to random via failures, we first discard wafers which have failed catastrophically (i.e., where more than half of the via chains are bad). Then, using data from the three PCM patterns that were used in Pilot Line III (s2v, s2vp, and se1p), we can make a rough estimate of via yield. We assume that a failed via chain contains only one bad via. Table 6 shows the estimate of yield.

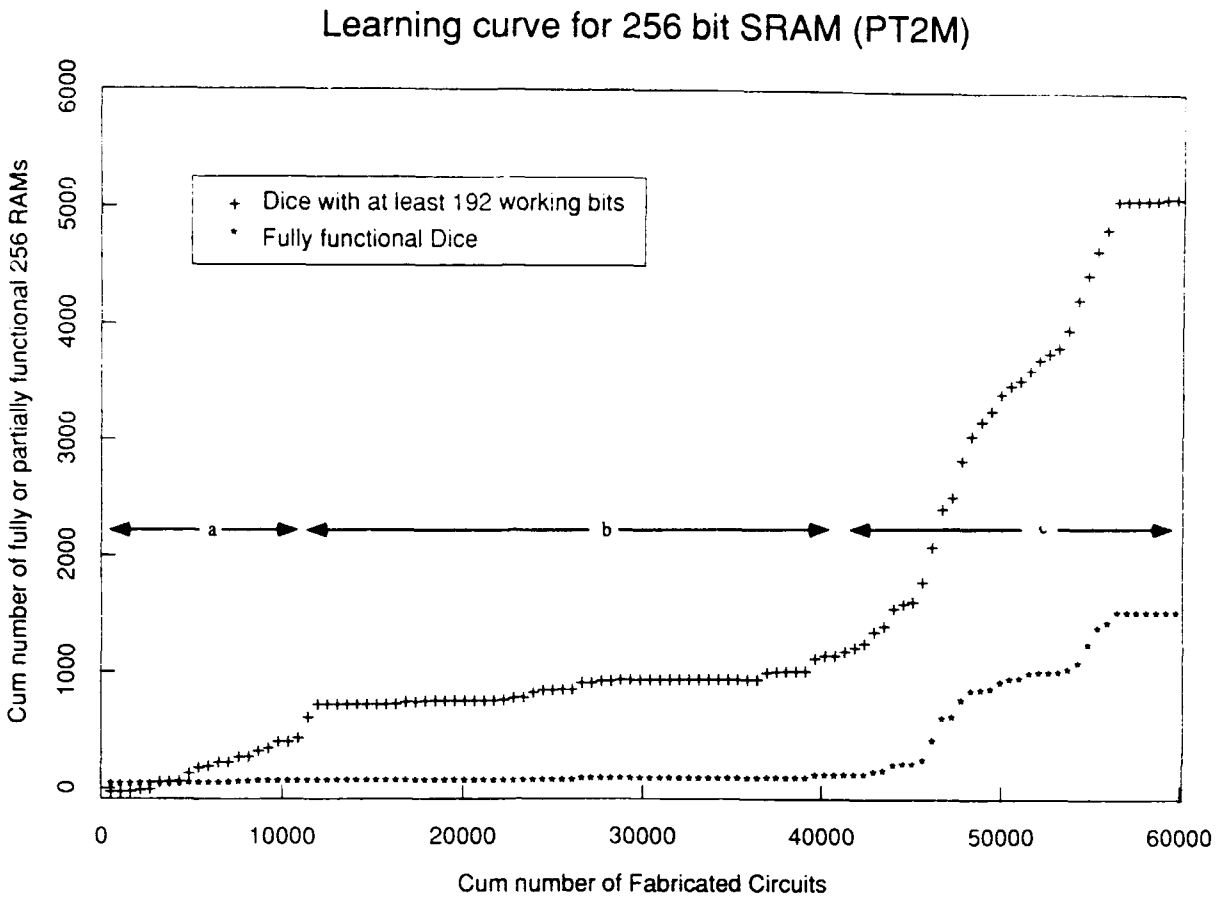
TABLE 6 — Estimate of Via Yields

	s2v (1988)	s2vp (1989)	se1p (1990)
Total Via Chains	3870	2709	1772
Bad Via Chains = Number of Bad Vias	164	139	47
Probability of One Via Being Bad	9.9×10^{-6}	1.2×10^{-5}	6.2×10^{-6}
Probability of a Good Circuit with 100,000 Isolated Vias	0.37	0.30	0.54

The last line of the table shows the expected yield due to defective vias in 4K SRAM I, where there are about 100,000 isolated vias.

Learning Curves

To evaluate our "learning," we studied the progress of the PT-2M memory (110 wafers fabricated). In Figure 4 (top), we plot the cumulative number of partially or fully functional circuits vs. the total number of fabricated circuits. There are three regions of interest: (a) the early part where we learn quickly to fabricate partially working circuits but few are fully functional; (b) the flat area where problems appear and the learning slows down; and (c) the fast ramp where the problems of region (a) have been resolved through aggressive failure analysis and Statistical Process Control. These three regions are related to the history of the E/D ratio, a parameter we have previously shown to be a key predictor of memory performance. (E/D ratio is the ratio of EFET and DFET currents.) Figure 4 (bottom) shows the E/D ratio. When E/D < 1, good memories can be made (regions (a) and (c)). When we lost control of the E/D ratio, and it became greater than 1, we could not make good memories (region (b)). This same information is shown in control chart form in Figure 5. The flat portion of Figure 4 (top) corresponds to the center of Figure 5, where sigma (the within-wafer standard deviation of the E/D ratio) is large.


Learning curve for 256 bit SRAM (PT2M)
Dice with at least 192 working bits
Fully functional Dice
Cum number of fully or partially functional 256 RAMs
Cum number of Fabricated Circuits
a
b
c
0
1000
2000
3000
4000
5000
6000
0
10000
20000
30000
40000
50000
60000

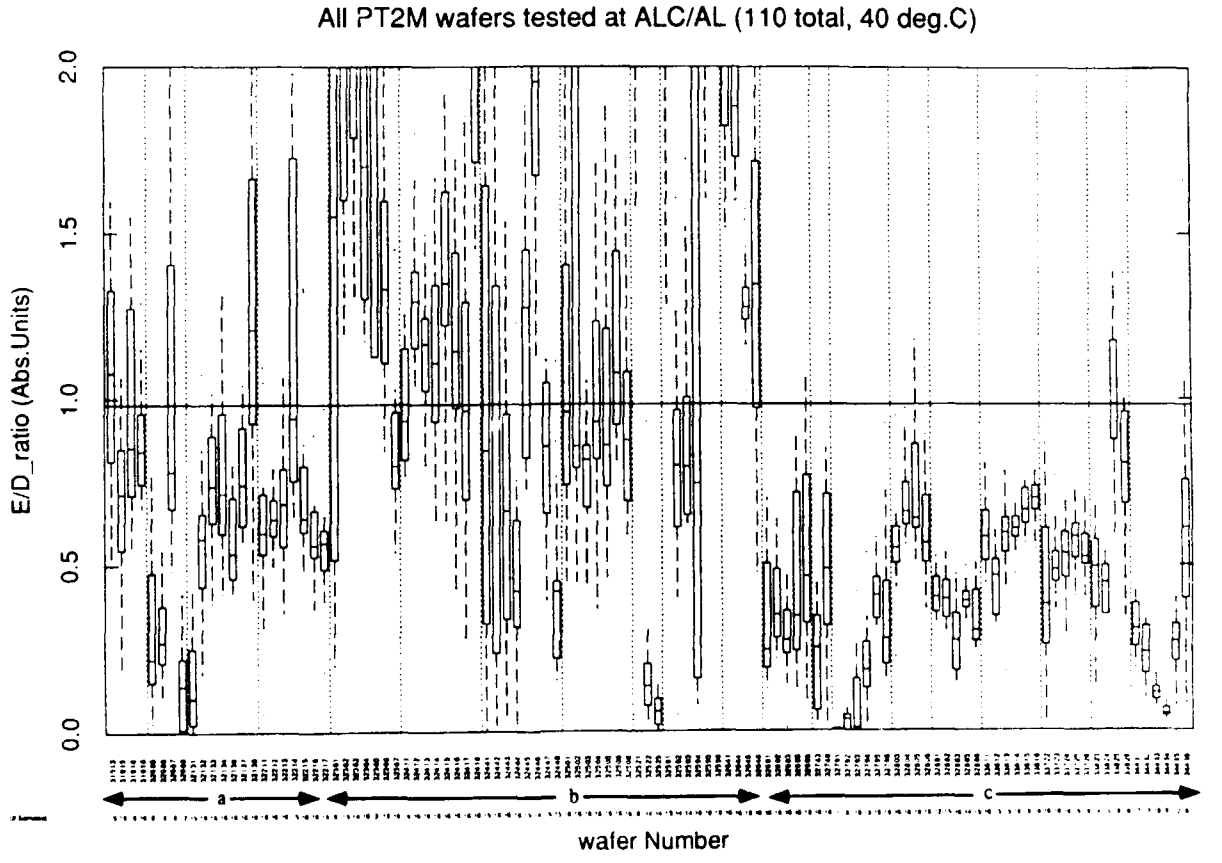
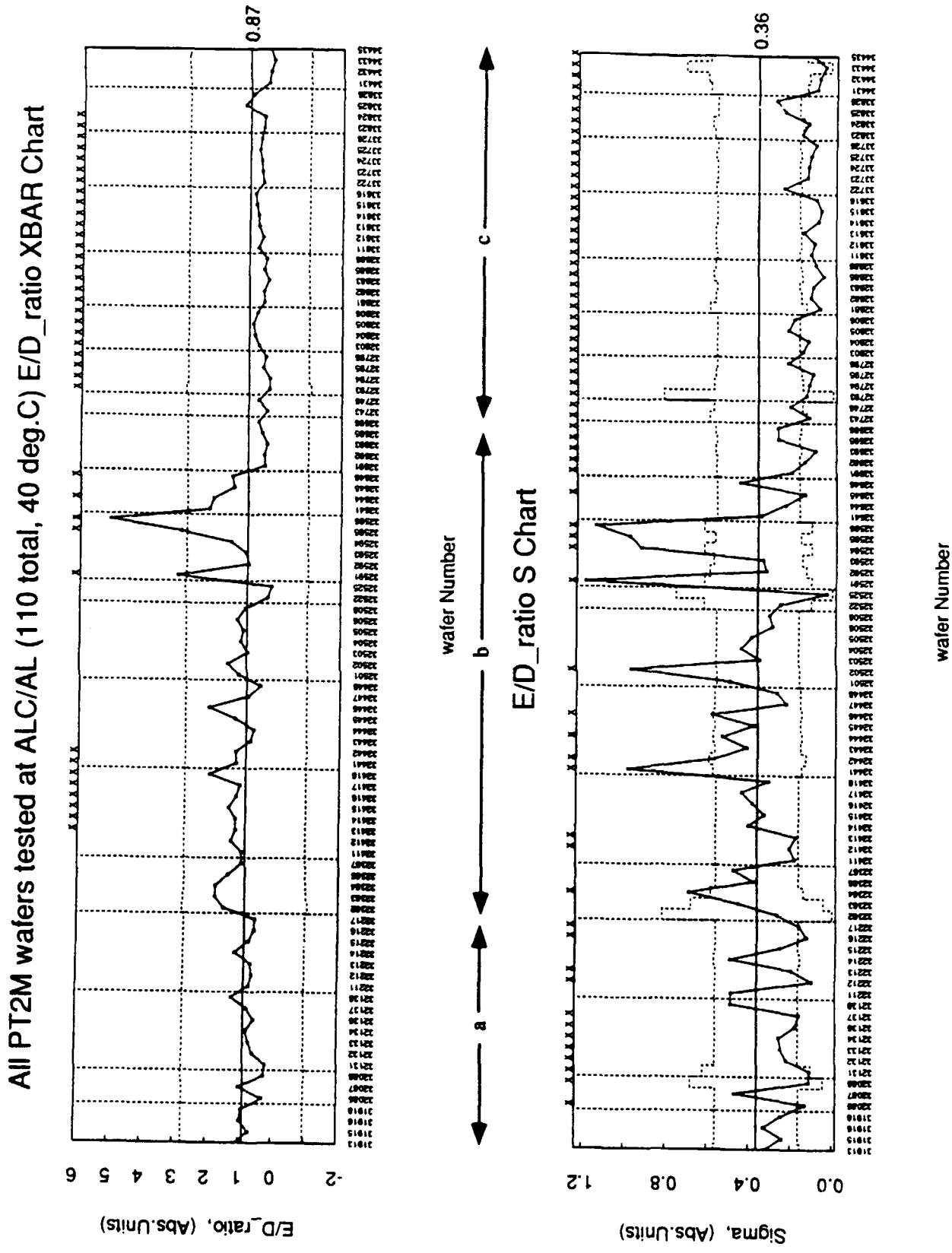

All PT2M wafers tested at ALC/AL (110 total, 40 deg.C)
E/D_ratio (Abs.Units)
wafer Number
a
b
c
0.0
0.5
1.0
1.5
2.0

Figure 4.



$\bar{X}$ - s Chart for PT-2M E/D Ratio

Figure 5.

3. PILOT PRODUCTION

3.1 MBE Operation (H-H Vuong, C. W. Ebert, E. L. Yachera)

From October 1990 until the present, the MBE wafer manufacturing area delivered 100% of the product requirement for the whole GaAs line without any interruption. The total number of production wafers grown on all three MBE machines is 1065, not including wafers with experimental structures, from October 1990 through March 1991. The number of production wafers grown in this period is lower than our capacity because of the reduced demand in the fourth quarter of 1990. Of these 1065 wafers, 921 wafers met all shipping specifications, giving an overall yield of 86.5%. Of all the wafers grown, 337 were of the Pilot Line III structure, with 313 wafers meeting all shipping specification, giving a yield of 93%. These results show that the MBE facility is fully capable of meeting production requirements, producing wafers at a high yield especially for the HFET structure used for the Pilot Line.

The yield figures represent a good improvement over the previous period. From April 1990 through September 1990, the overall yield was 72%, and the yield for the structure used by the Pilot Line was 78%. This "learning curve" improvement is due mainly to the increase in experience of our operators, and their attention to keeping each part of the MBE process highly consistent from one batch to another. It was facilitated by the continuous recording of the reasons for scrapping wafers, and the subsequent loss analysis which points out areas for improvement. Our yield improvement was also helped by running the MBE machines closer to true production mode by growing the same structure for as long as three weeks at a stretch. This and other improvements were made by our operators at the regular MBE Quality team meetings.

In addition to the shipment against request and the yield, our third quality metric is machine uptime. In the previous period, this averaged 70%. There is a slight improvement from October 1990 until present, with a new average uptime of 75%. The new uptime would have been even higher except for a large planned downtime at the end of 1990 which was set aside for major machine improvements. Another way of measuring the reliability of the MBE machines is the frequency of downtime caused by unplanned maintenance. This has improved over the last two years, through analysis of the cause for machine failure and subsequent component redesign and preventive maintenance to reduce or avoid a repeat failure from the same cause (see Table 7).

TABLE 7 — Frequency of Unplanned Maintenance For MBE1 and 2 for 1989 and 1990

Machine	1989	1990
MBE1	4	1
MBE2	5	1

Note: Machine 1 was not fully operated from
April to September of 1990 because of lack of operators.

In 1991, up until the present, only one unplanned maintenance has occurred. The cause of this failure, an accidental turn-off of the main pump, has been addressed through the addition of the guard for this and similar switches.

During this time period, we made several major improvements to our MBE machines. One is retrofitting two of the three machines with new vacuum steel pipes for the Liquid Nitrogen cooling. This will facilitate the procedure during the source reloads. Secondly, all machines are

now fitted with the dual-zone source furnaces for the Ga sources. This change together with greater attention to detail in both the substrate preparation and the wafer transfer steps have enabled us to reduce the defect density of all structures to their lowest levels so far. To date, the lowest defect density is 16 cm^{-2}, and typical wafers have fewer than 100 cm^{-2}.

3.2 Pilot Line Throughput, Interval & Yield (J. H. Duchynski, S. M. Parker)

During the last six months, 84 wafers were started in Pilot Line III. Starts were made in the baseline SARGIC-SA technology (see Section 3.3) for the following codes: 4K SRAM II, Cell Array Casino Test Chip, and 32-Bit Multiplier. Before the end of March, eleven wafers completed processing and were PCM tested. The others have not yet completed processing. This lower level of Pilot Line wafer fabrication activity resulted from the Vth Quality Team's suspension of lot starts for part of the reporting period while the EFET etching difficulties were being resolved. Table 8 summarizes the starts and completions by code for this reporting period. For comparison, there were 260 wafer starts and 127 completions in other AT&T SARGIC codes.

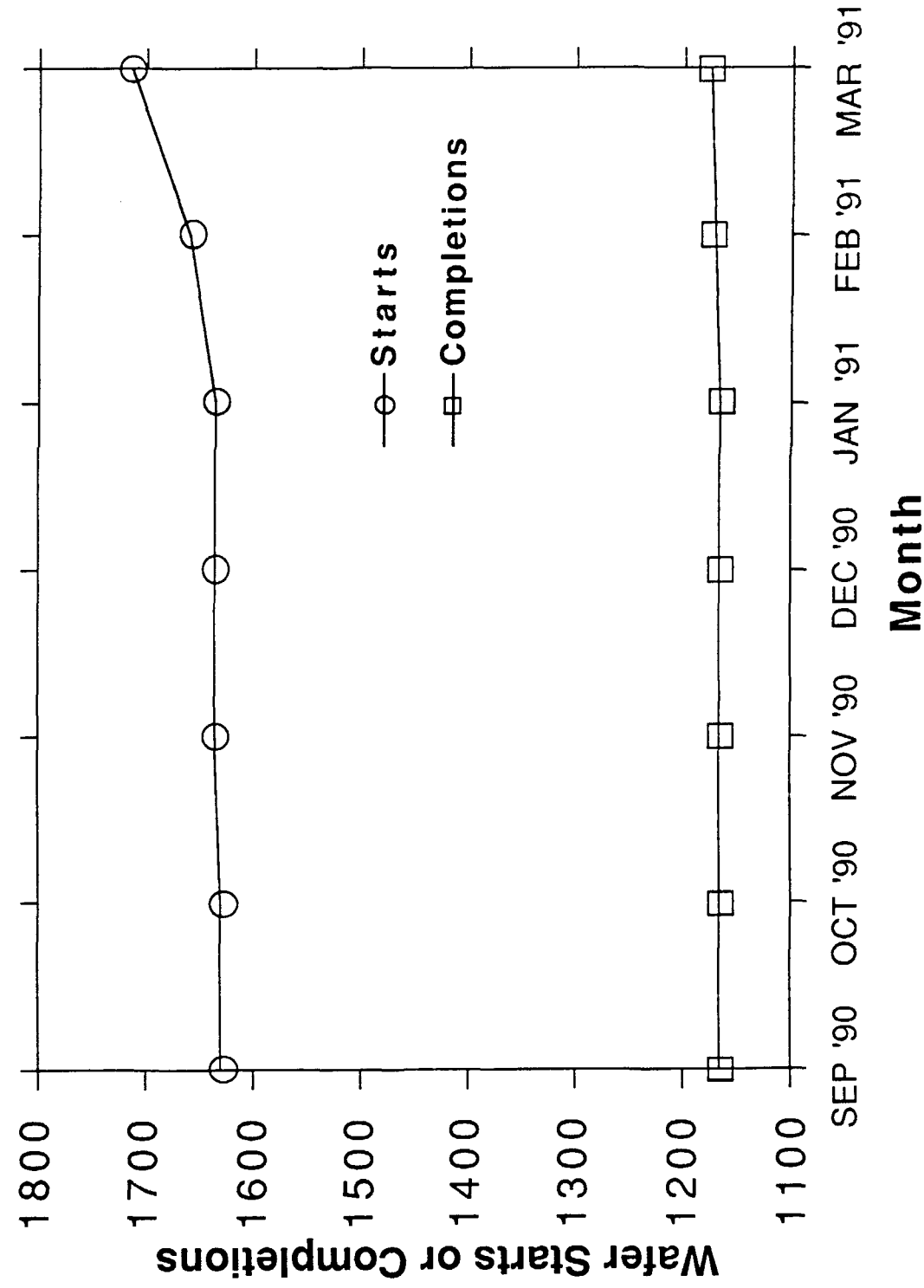
TABLE 8 — Pilot Line Activity

Code Name	Wafers Started	Wafers Completed
4K SRAM II	36	6
Cell Array Casino Test Chip	24	0
32-Bit Multiplier	24	5
	84	11

The cumulative Pilot Line wafer starts and completions through fiscal March, 1991, are shown in Figure 6. A total of 1714 wafers have been started and 1177 wafers have reached completion. Additional wafers were started on the Pilot Line for other AT&T projects which involved SARGIC as well as recessed gate technologies. As of the end of March, 1991, total cumulative starts across all technologies were well above 4500 wafers, and more than 2850 wafers have been completed through PCM testing. Wafer starts combined for all projects averaged 31 wafers/week for this reporting period. Of this total, Pilot Line starts averaged 3.4 wafers/week while the other SARGIC starts averaged 10.4 wafers/week.

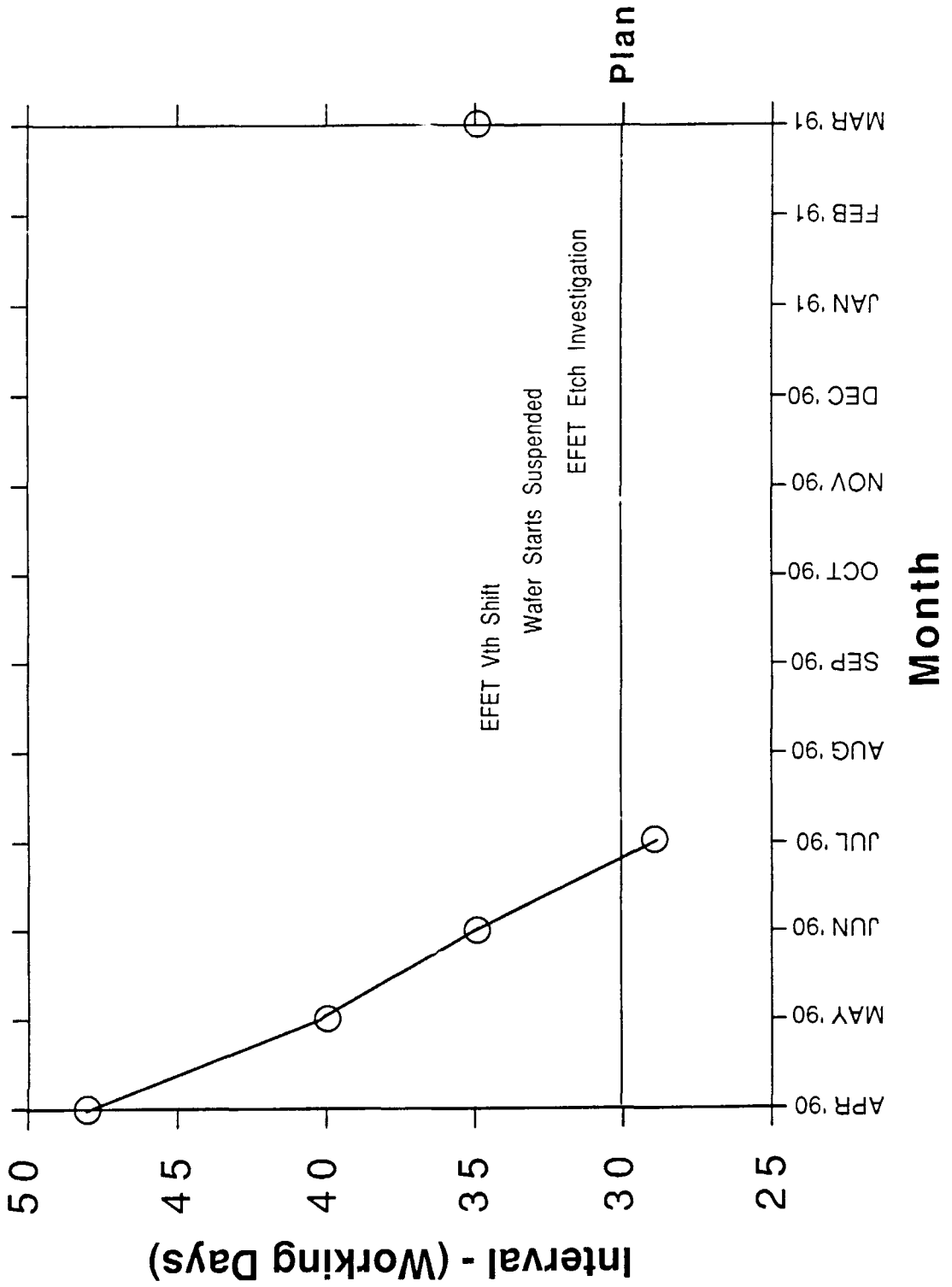
The computed fabrication interval for the Pilot Line codes during the past 12 months is shown in Figure 7. This interval represents the sum of the average intervals of the individual process steps which are active each month. The average computed interval for April through July, 1990, was 38 working days. No intervals were reported for August, 1990, through February, 1991, due to the low level of activity in the line which resulted from the suspension of wafer starts during the EFET etch investigation. The next meaningful interval calculations occurred in March, 1991, where the average computed interval was 35 working days. The average actual fabrication interval for the two lots reaching completion in March was 34 working days.

An additional indication of the Pilot Line's level of activity can be measured in terms of "wafer moves" per week. The wafer fabrication line is divided into 34 process zones. A "wafer move" is the movement of one wafer through one process zone. A comparison of the average wafer moves per week for the Pilot Line codes and the other SARGIC codes has been plotted in Figure 8 for



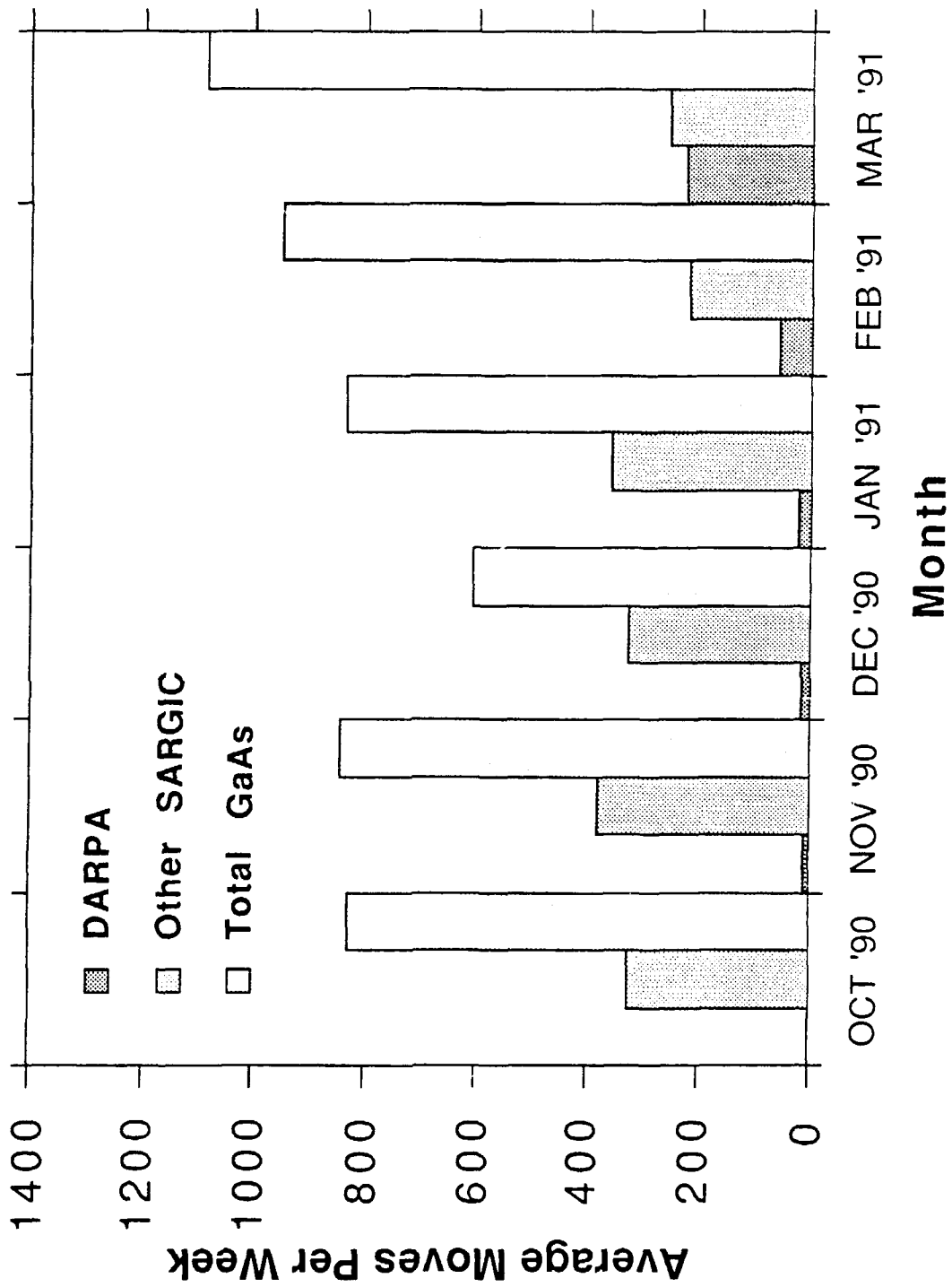
Pilot Line III Wafer Fab Cumulative Starts and Completions
(Pilot Line Codes)

Figure 6.



Pilot Line III Wafer Fab Interval
(Pilot Line Codes)

Figure 7.



Pilot Line III Wafer Fab
Average Moves Per Week

Figure 8.

the current reporting period. The total wafer moves per week across all GaAs technologies is plotted as well. During the past six months, the total level of wafer fabrication activity has averaged 857 moves/week across all technologies. Of this total, 311 moves/week were made on average with the non-Pilot Line SARGIC codes. These other SARGIC codes primarily utilized the EFET-only or DFET-only technologies. The first substantial activity for the Pilot Line codes occurred in March, 1991, when the average wafer moves per week jumped to 224. This represented 21% of the total line activity for that month.

Figure 9 shows the wafer fabrication yield for the Pilot Line codes during the past 12 months. This is a mechanical yield which compares the number of wafers which successfully complete each active processing zone to the number of wafers originally started at each of those processing zones. For most of the previous six month reporting period, the yield fluctuated around 86%. There wasn't any fabrication activity directly on any Pilot Line lots in October, 1990, and so no yield number could be reported. For the most recent five months, the fabrication yield has averaged 95%. However, the Pilot Line activity level was extremely low from November, 1990, through February, 1991. Thus, the most meaningful yield calculation occurred in March, 1991, when the DARPA activity level increased again. For March, the wafer fabrication yield was 92%.

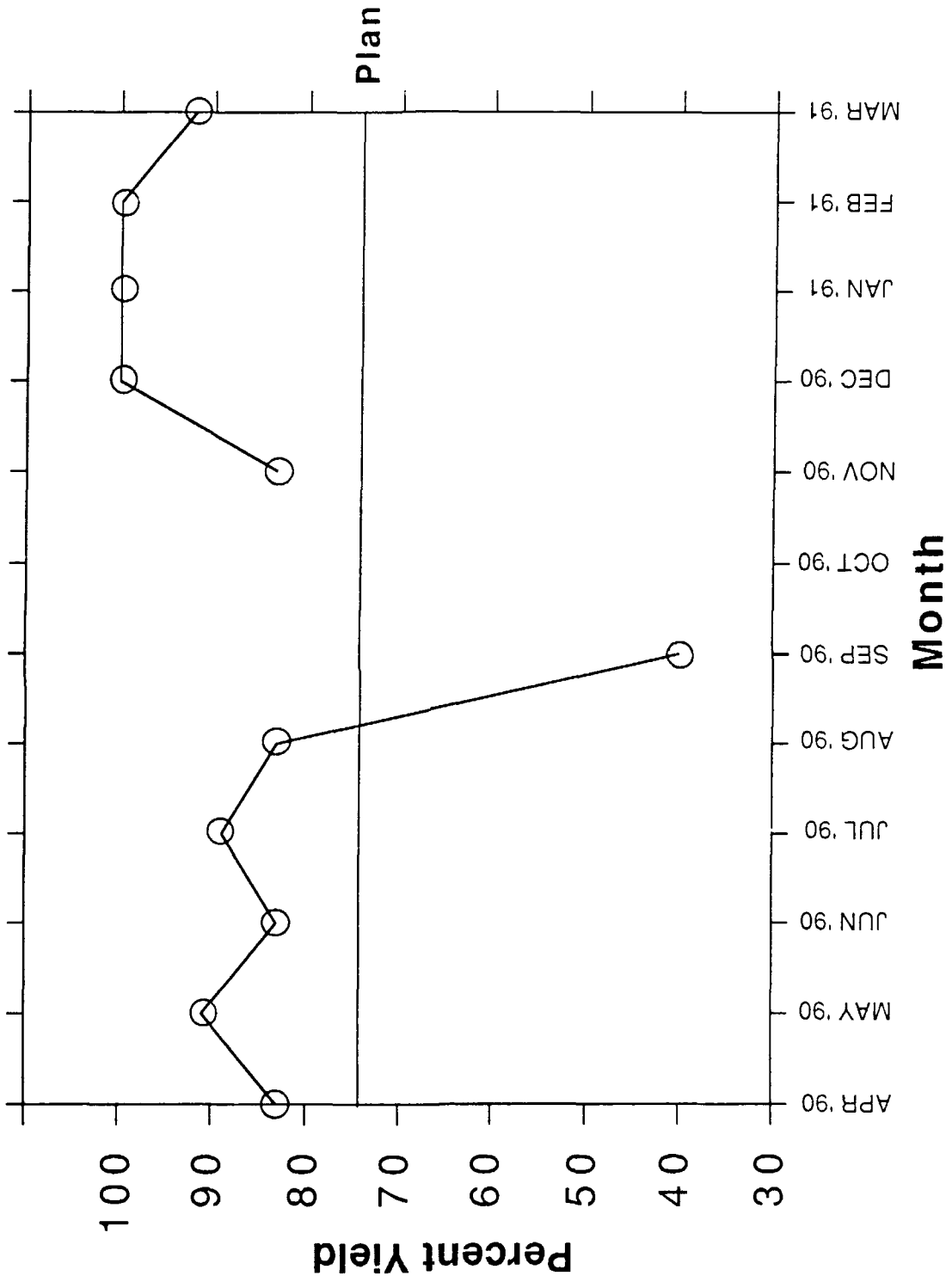
3.3 Baseline Technology (C. L. Reynolds, A. D. Brotman, S. F. Nygren)

In the previous report, we demonstrated that the ED11 MBE structure produces FETs much closer to target electrical parameters than ED10, so ED11 was introduced into the Pilot Line as the standard process. Initially, the production ED11 wafers performed the same way as the experimental ED11 wafers. Then we saw a sudden increase in the EFET threshold voltage and diode voltage of about 100 mV. The DFET characteristics were not affected. We quickly examined the obvious possible causes for threshold shift (e.g., MBE layer thickness and doping, furnace anneal process), but we found no problems with them. We therefore suspended wafer starts and initiated a more extensive failure analysis.

Scanning electron microscope examination of device wafers suggested improper etching of the AlGaAs etch stop layer during formation of the EFET tub. These results were confirmed by transmission electron microscopy (TEM) and static secondary ion mass spectrometry (static SIMS). TEM observations revealed the presence of a non-uniform AlGaAs layer under the WSi gate, while static SIMS showed AlGaAs in the EFET tubs immediately prior to gate deposition. Data in the literature indicate that the Schottky barrier height of a metal on AlGaAs increases from ~0.65 V to 0.9V as the Al fraction increases from 0 to 0.5. We concluded that AlGaAs remaining in the EFET tubs was the source of the threshold voltage problem. Wafers fabricated with an EFET-only process (that is, no DFET layers and no tubs) had the same threshold voltages as the original experimental ED11s. This also supports the above conclusions about residual AlGaAs in the EFET tubs.

On the basis of etching studies, we determined that the problem was related to the KI/I_2 etchant, so we sought a replacement. As reported previously, the PA (NH_4OH and H_2O_2) and PP (H_3PO_4 and H_2O_2) etches were more effective than KI/I_2 in removing AlGaAs in the EFET tubs. The PA etch is advantageous because it has different etch rates in GaAs and AlGaAs, while the PP etch has the advantage of being used in other GaAs wafer fabrication and being automated.

As of the last report, we were awaiting electrical data using our SARGIC-SA process from nine lots in which the tub etchant was split among KI/I_2, PA, and PP. The SARGIC-SA process is



Pilot Line III Wafer Fab Mechanical Yield
(Pilot Line Codes)

Figure 9.

used for other AT&T wafer fabrication and is similar to the process used in all previous Pilot Line lots (SARGIC-S). The SARGIC-SA process differs in two ways from SARGIC-S. It uses 1) a bilayer WSi/W gate metallization and 2) a higher (1.5E14 vs. 1E13 cm^{-2}) dose for deep isolation implant. The bilayer gate metal has lower gate metallization resistance, which may be beneficial and certainly won't be detrimental. An advantage of the SA isolation dose is that it prevents a rapid increase in leakage at higher voltages. Also, the SA implant provides the same reduction in sidegating as the S implant. On the other hand, the higher dose SA process causes ten times the leakage current (30-40 nA at 3V rather than 3-5 nA) for two 75 μm ohmic pads separated by 2 μm. Leakage currents of this magnitude are not important in our circuits, and further, this combination of geometry and bias are unlikely in actual circuits. An additional concern for the SA process is that the higher dose deep isolation implant must be done outside the clean room, with potential risk for increased particulate contamination. However, the implant machine is one which is used occasionally for other GaAs wafer fabrication and has been used previously for Pilot Line fabrication without adverse consequences. Data on PT-2M memories for which the wafers were implanted both inside and outside the clean room indicate no yield differences. Thus, we conclude this is not a problem. Taking all these issues together, we chose to use the SARGIC-SA process for all future Pilot Line wafer fabrication. There are no serious disadvantages, and the advantages are significant: all electrical data describing the new etch process came from SA wafers. Also, this is the appropriate time to consolidate two process variations into one.

The electrical data on the nine experimental lots split among the different etches support the results from our etching studies. Where the original process with KI/I_2 yields EFET threshold voltages which are −100 mV too positive, the wafers fabricated with either the PA or PP etches have threshold voltages and currents near target. Since use of the KI/I_2 etchant is unacceptable, the real question was whether to choose PA or PP. Of the nine split lots, each contained two or three wafers etched with PA and PP so that a total of 14 wafers of each etchant successfully reached BOTMET testing, the first electrical test in our process. We censored the data to remove default values and fictitious data. Then, for each electrical parameter of interest, we plotted the data as an $\bar{X}$-s control chart. Any wafers shown to be satistically out-of-control were discarded from the data set so that we could analyze data representative of a process in control. An example of the data analysis process is shown in Figures 10 and 11. The top half of Figure 10 shows an $\bar{X}$ plot for EFET current measured with Vgs=0.5 V.† Each point is the average value for a specific wafer, and all points are in control. The bottom half of Figure 10 is an s plot; the intra-wafer standard deviation is plotted for each wafer. Five points are out-of-control (denoted by x's along the top edge of the plot), and wafer 37203 has an unusually high standard deviation. When wafer 37203 is deleted from the data set, we get the plot in Figure 11, in which all points are now in control. In examining other relevant parameters, no other wafers need to be eliminated.

Table 9 shows the channel currents obtained from these wafers. It also shows the average intra-wafer variations of these currents (sigma). In all cases, the data are BOTMET data corrected to predict the values that would be obtained at final test.

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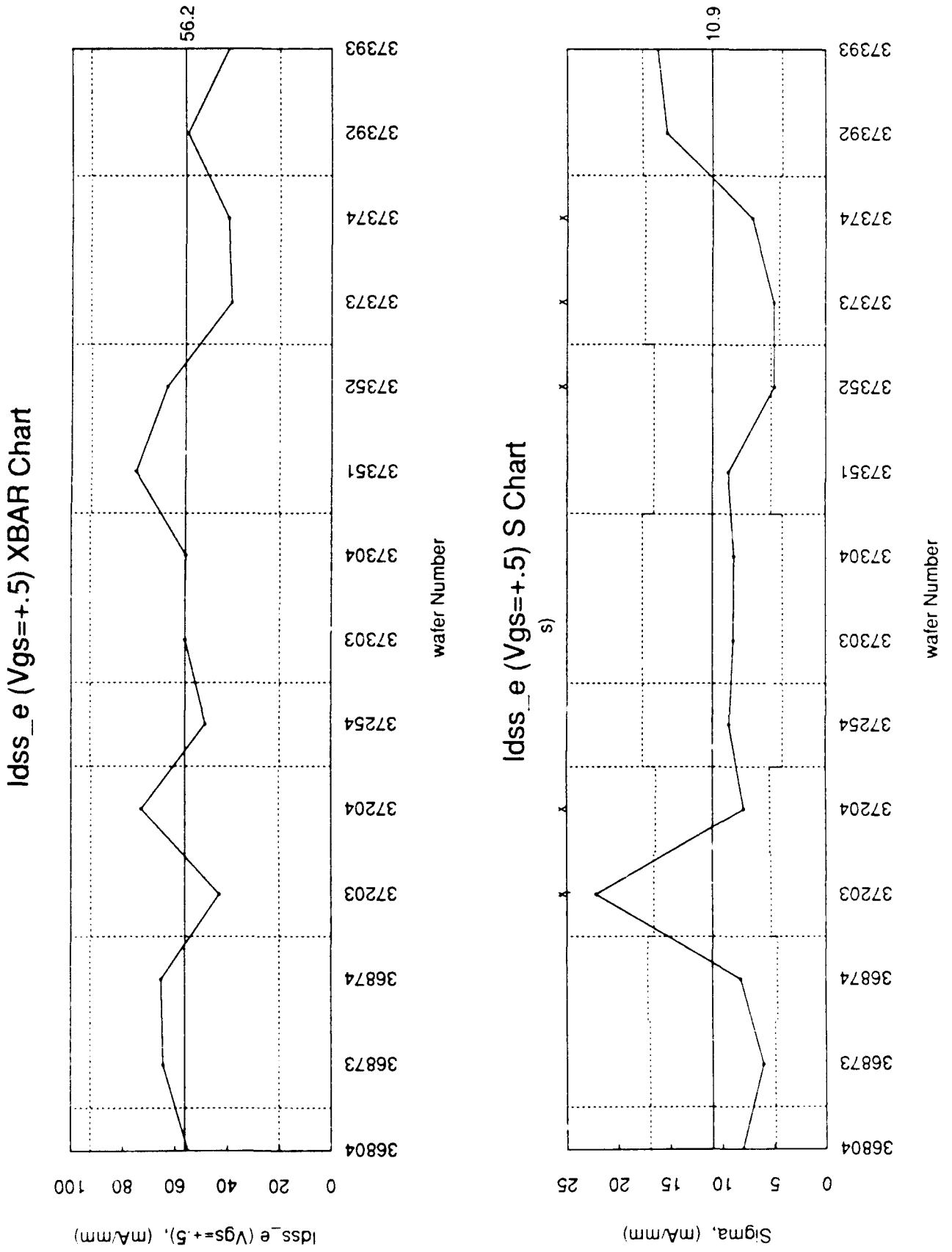
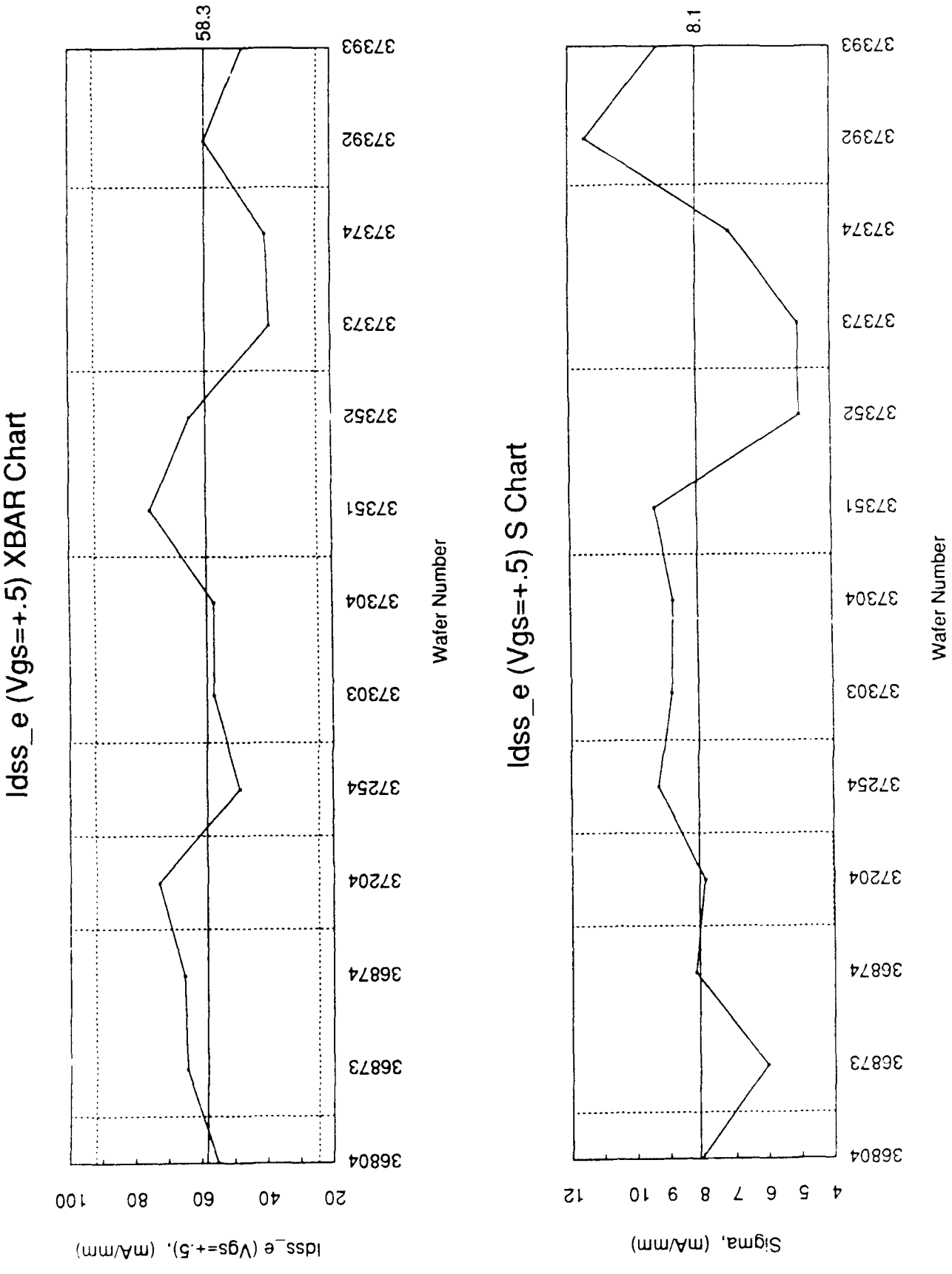
† In the past, we focused primarily on threshold voltage as our figure of merit; however, we now tend to use channel current at Vgs=0.5 V and 0 V for the EFET and DFET, respectively. A definition of threshold voltage becomes problematic at high values and also depends on the softness of turn-on.



$\bar{X}$ - s Chart for EFET Ids (PA Etchant)

Figure 10.



$\bar{X}$ - s Chart for EFET Ids (PA Etchant)
(out of control points removed)

Figure 11.

TABLE 9 — Predicted Current at Final Test

	EFET Current (mA/mm)		DFET Current (mA/mm)	
	Mean	Sigma	Mean	Sigma
Target	55	—	85	—
PA	51.1	6.8	86.8	12.8
PP	56.7	9.0	86.9	16.1

On the basis of the data in the table, both etchants produce the same average value for DFET current, which is close to target. The intra-wafer standard deviation is slightly larger for wafers fabricated with the PP etch. For EFETs, PP seems to provide currents closer to target. A two-way analysis of variance shows that PP gives a current significantly different statistically from PA, but within-wafer and wafer-to-wafer variations overwhelm the effects of etchants.

In the end, we chose the PP etchant for the final Pilot Line lots. It is closer to target and is preferred from a manufacturing point of view. The use of the SARGIC-SA process also consolidates two of AT&T's processes into one.

EFET SCALING

In addition to solving the EFET threshold problem, the PA and PP etches also solve the previously reported EFET scaling problem. That is, key EFET electrical parameters are now essentially constant over a wide range of EFET widths. Scaling data for typical EFETs processed using the PP etch is shown in Table 10.

TABLE 10 — EFET Scaling Data

wafer	type	width mm	Ids mA/mm	Vg(Ids=10mA/mm) mV	Vg(Ids=50mA/mm) mV	Vf(Ig=10mA/mm) mV
37306	e	.002	42.761	239	545	683
37306	e	.005	52.781	206	484	687
37306	e	.010	51.157	213	493	695
37306	e	.025	53.71	194	479	705
37306	e	.050	52.991	194	483	711
37306	e	.100	49.505	208	503	732
37306	e	.150	50.273	209	498	753
37306	e	.200	49.079	208	505	781

Ids (Vgs=0.5V, Vds=2.5V) is drain current.
Vg (Ids=10 or 50 mA/mm, Vds=2.5V) is gate voltage.
Vf (Ig=10 mA/mm, Vds=0V) is diode forward voltage.

It can be seen that devices from 5 μm to 200 μm scale very well. In contrast, with KI/I_2, there was a 100 mV shift in Vg when device width changed from 3 μm to 50 μm. In Table 10, the increase in Vf for large devices is due to gate metal resistance and is included in the device design model.

4. RELIABILITY & QUALITY

4.1 Reliability Testing (P. F. Thompson)

HTOB-1

The first 1000-hour PT-2M memory High Temperature Operating Bias (HTOB) test has been completed. Seventy-nine devices were placed on test: 26 at 150°C, 27 at 175°C, and 26 at 200°C. Eight additional devices were used as controls. Chips were taken from two wafers and assembled into 44-lead ceramic packages. A non-hermetic lid-attach was used. All tested and control devices were fully functional, with 256 working bits in both pipeline and ripple modes and an operating speed of at least 200 MHz. Devices were statically biased during HTOB. At 16, 32, 64, 128, 256, 600, and 1000 hours, devices were removed from reliability testing and electrical characterization was performed. After the 1000 hour electrical characterization, failures were inspected and lifetime parameters determined.

Bit loss was used as the failure criterion, with failure statistics being determined for 1, 10, and 26 lost bits. (26 is 10% of the 256 bits.) While the loss of one bit indicates a failed memory, we believe a single bit loss is not an accurate indicator of reliability statistics. The 256-bit PT-2M memory is a preliminary design. One known weakness is the propensity for bit flipping, and another problem is sub-threshold current. These and other early design weaknesses have been addressed in the newest memory design (4K SRAM II). Failure criteria from one bit to 10% bit loss were used to determine lifetime. The intent of the HTOB test was to gauge reliability of the digital technology, and not to examine the reliability of the preliminary PT-2M design in particular.

Relative changes in electrical parameters, such as Vgs (an equivalent gate-drain voltage), VddMn (minimum supply voltage for the part to work) and Idd (total current), were considered as possible failure criteria, but these parameters did not change in a consistent manner. There were no statistically significant differences in parameter changes between failed and good devices and between control and failed devices. In addition, the changes were extremely small (typically less than one percent), even in the case of 10% bit loss.

Electrical test data for the eight control devices remained stable through 600 hours. No bits were lost, and electrical parameters showed no statistically significant changes. One thousand hour data for the controls are not yet available.

All failed devices were delidded and visually inspected at 200X. There were no signs of physical damage, electromigration, etc. Such a result is not surprising, since the parametric changes were generally gradual.

Lifetime parameters were calculated with the assistance of STAR (STatistical Analysis of Reliability), an AT&T software package. The lognormal distribution (Equation 1) was used to model failure behavior. In Equation 1, T_{50} refers to the median lifetime, and σ is the shape parameter for the lognormal distribution.

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} \exp\left[-(1/2\sigma^2)\,(\ln t - \ln T_{50})^2\right] \qquad (1)$$

Median lifetimes from the three test temperatures are used with the Arrhenius relation (Equation 2) to determine the activation energy (E_a) and the constant C. k is Boltzman's constant, and T is temperature in K.

$$T_{50} = C \exp\left[E_a/kT\right] \quad (2)$$

Once T_{50} for one temperature and E_a have been calculated, T_{50} for any desired temperature can be found from Equation 2.

Table 11 contains MTTF, E_a and σ values for 65°C ambient, for each bit loss criteria considered.

TABLE 11 — PT-2M Reliability Results for Different Bit Loss Criteria

# bits	MTTF	E_a (std dev)	σ (std dev)
1	1.5×10^5	0.64(0.15)	1.30(0.15)
10	2.0×10^6	0.88(0.18)	1.01(0.15)
26 (10%)	2.0×10^6	0.86(0.18)	1.07(0.16)

E_a for electronic devices typically falls in the range of 0.7-1.7eV. As σ increases, the maximum failure rate increases and moves towards smaller time, and the distribution becomes less symmetrical. For a σ of about 1.0, peak failure rate is well before T_{50}, with a relatively large tail (asymmetry) to large times. The standard deviation for E_a and sigma are contributed to by the sample sizes, missing test data, and the nature of the preliminary PT-2M design. For ten percent bit loss at an operating temperature of 65°C, T_{50} is 1.96×10^6 hours (224 years), and the maximum failure rate over ten years is 75 FITs at ten years. In comparison, for AT&T GaAs lightwave codes, maximum failure rate is 40 FITs at 65°C ambient during a ten year life.

HTOB-2

The second 1000-hour PT-2M HTOB test is currently being electrically characterized after 100 hours aging. This is the first of four intervals (100, 200, 500, 1000 hours) for electrical characterization.

4.2 Designed Experiment: Furnace Anneal (T. C. Henry)

Introduction

Installation of a new high temperature GaAs anneal furnace was completed at the end of the second quarter of 1990. Initial development work focused on establishing a process recipe that would replicate the "old" furnace anneal process. Process optimization studies, using the design of experiments (DOE) methodology, were initiated after the initial process recipe was developed. The overall objective of the studies was to establish furnace operating conditions that would result in acceptable device characteristics and minimize the variation in the results. DOE techniques were incorporated in the work to use our resources more efficiently and minimize the time of the development cycle.

A three pronged sequential experimental approach was used to optimize the anneal process. In the first experiment, relevant process variables and reasonable operating ranges were identified by activating blanket silicon implants in LEC GaAs with a wide range of furnace conditions. The variables and operating ranges found to be important were used in the design of the second experiment. The objective of the second experiment was to develop a functional relationship between SARGIC EFET device characteristics and the furnace variables. Optimal operating conditions were chosen from models developed from the experimental data. In the third experiment, the variable range was further reduced around the optimal operating condition to examine the sensitivity of device results to smaller variations in the furnace variables.

Experiment 1

The first experiment was designed to identify the furnace variables that had an effect on implant activation and surface quality. The parameters varied in the experiment included anneal temperature, time, arsenic temperature, wafer position in the furnace boat, and hydrogen flow rate. LEC GaAs wafers were first implanted with a silicon dose of 3E12 ions/cm^2 at an energy of 160KeV, and then annealed in the furnace with various treatment conditions. Eddy current sheet resistance measurements were made on the wafers to evaluate implant activation and qualitative observations were used to gauge surface quality.

DOE techniques were used to choose the treatment conditions.† With five independent variables, and two set-points for each one, it would take 32 experimental runs to try all possible combinations. A properly designed experiment, however, gathers the same information from only 16 runs. The only risk in a designed experiment is possible ambiguity between some interactions, but the experiment is designed so that this is unlikely. Table 12 shows the treatment conditions for this experiment. For any given variable, half the treatment conditions use one set-point, and the other half use the other set point. This allows the subsequent analyses to include process variation in the process model. A seventeenth treatment condition is a centerpoint: all the variables are set midway between the setpoints used in the other treatment conditions.

The results indicated that the anneal temperatures, times, and arsenic source temperatures had a significant effect on implant activation and surface quality. Neither the gas flow rate nor wafer position in the furnace boat affected activation or surface quality. The results showed that the range of anneal and arsenic source temperatures should be adjusted for the device wafer experiment to improve surface quality and activation uniformity. The lower arsenic temperature limit was increased from 380°C to 390°C to avoid the surface degradation observed with 850°C anneals. The anneal temperature lower limit was also increased slightly to obtain greater activation and improve uniformity.

† See, for example, William J. Diamond, 1989, *Practical Experimental Designs for Engineers and Scientists.* Second edition. New York: Van Nostrand Reinhold.

TABLE 12 — Experiment 1 Treatment Conditions

Treatment Number	Temperature (°C)	Time (min)	Flow Rate (l/min)	Boat Position	Arsenic Temperature (°C)
1	775	5	0.5	40	380
2	850	5	0.5	10	380
3	775	30	0.5	10	380
4	850	30	0.5	40	380
5	775	5	2.5	10	380
6	850	5	2.5	40	380
7	775	30	2.5	40	380
8	850	30	2.5	10	380
9	775	5	0.5	10	430
10	850	5	0.5	40	430
11	775	30	0.5	40	430
12	850	30	0.5	10	430
13	775	5	2.5	40	430
14	850	5	2.5	10	430
15	775	30	2.5	10	430
16	850	30	2.5	40	430
Centerpoint	812.5	17.5	1.5	25	405

Experiment 2

The second experiment, which uses SARGIC EFET-only wafers, was designed to determine the relationship between device parameters and furnace independent variables. The furnace variables in the experiment included anneal temperature, anneal time, and arsenic temperature; the results of the first experiment indicated that the gas flow rate and wafer position in the boat were not significant variables, so they were not included in this experiment. This experiment required 14 treatment combinations plus six centerpoint replications to determine if any curvature was present in the process model. In this case, we used a more sophisticated experimental design. In addition to high and low setpoints for each variable, a few extra treatment conditions include extra-high, extra-low, or centerpoint values. This is shown in Table 13.

Device data were obtained when the wafers were tested after the passivation step. A statistical analysis was performed to relate the device characteristics to the furnace variables. Correlation coefficients which relate the fit of the data to the various device parameters were extracted and are illustrated in Table 14. A device parameter is considered to be significantly affected by the anneal process when the correlation coefficient between the data and the experimental variables is greater than 0.52. The significant device parameters, when evaluated with this criteria, included Ids, variance of Ids, Vi50, V_{diode}, R_N, R_{N+}, variance of R_{N+} sheet resistance, gm, variance of gm, R_{out} and variance of R_{out}.

TABLE 13 — Experiment 2 Treatment Conditions

Treatment Condition	Temperature (°C)	Time (min)	Arsenic Temperature (°C)
1	850	10	430
2	850	25	430
3	800	25	400
4	800	25	430
5	800	10	430
6	800	10	400
7	850	25	400
8	850	10	400
9	783	17.5	415
10	825	5	415
11	867	17.5	415
12	825	17.5	440
13	825	30	415
14	825	17.5	390
Centerpoint	825	17.5	415

TABLE 14 — Furnace Anneal Results for Experiment 2

Response	Correlation Coefficients	
Ids	0.70	Drain Current with Vgs=0.5V
Variance of Ids	0.57	
Ig	0.52	Gate Current with Vgs=2.5, Vds=0
Variance of Ig	0.42	
R_{out}	0.64	Output resistance with Vgs=0.5V
Variance of R_{out}	0.92	
gm	0.63	gm at Vgs=0.5V
Variance of gm	0.64	
R_{N+}	0.66	Sheet resistance of N+ layer
Variance of R_{N+}	0.59	
R_N	0.89	Sheet resistance of N layer
Variance of R_N	0.30	
Vi50	0.70	Vgs for drain current=50 mA/mm
Variance of Vi50	0.35	
V_{diode}	0.62	Vgs at Igs=10μA/μm, Vds=0
Variance of V_{diode}	0.48	

To relate device characteristics to furnace variables and to select optimal operating conditions, we developed a model from the experimental data. The model can be used to draw contour plots illustrating how annealing conditions affect FET parameters. Figure 12 (top) shows how Ids is

affected by anneal time and anneal temperature when the arsenic temperature is 425°C. Our goal is to locate an operating region where small changes in furnace operation product minimal changes in Ids. According to the model, as shown in Figure 12 (top), we should use a temperature of 835°C with a time of 22.5 minutes since that is the center of the flat region of the contour plot. Then small accidental changes in anneal conditions cause almost no change in Ids. That is, Ids remains constant within ±1-2% if 820 < temperature < 850°C and 20 < time < 25 minutes.

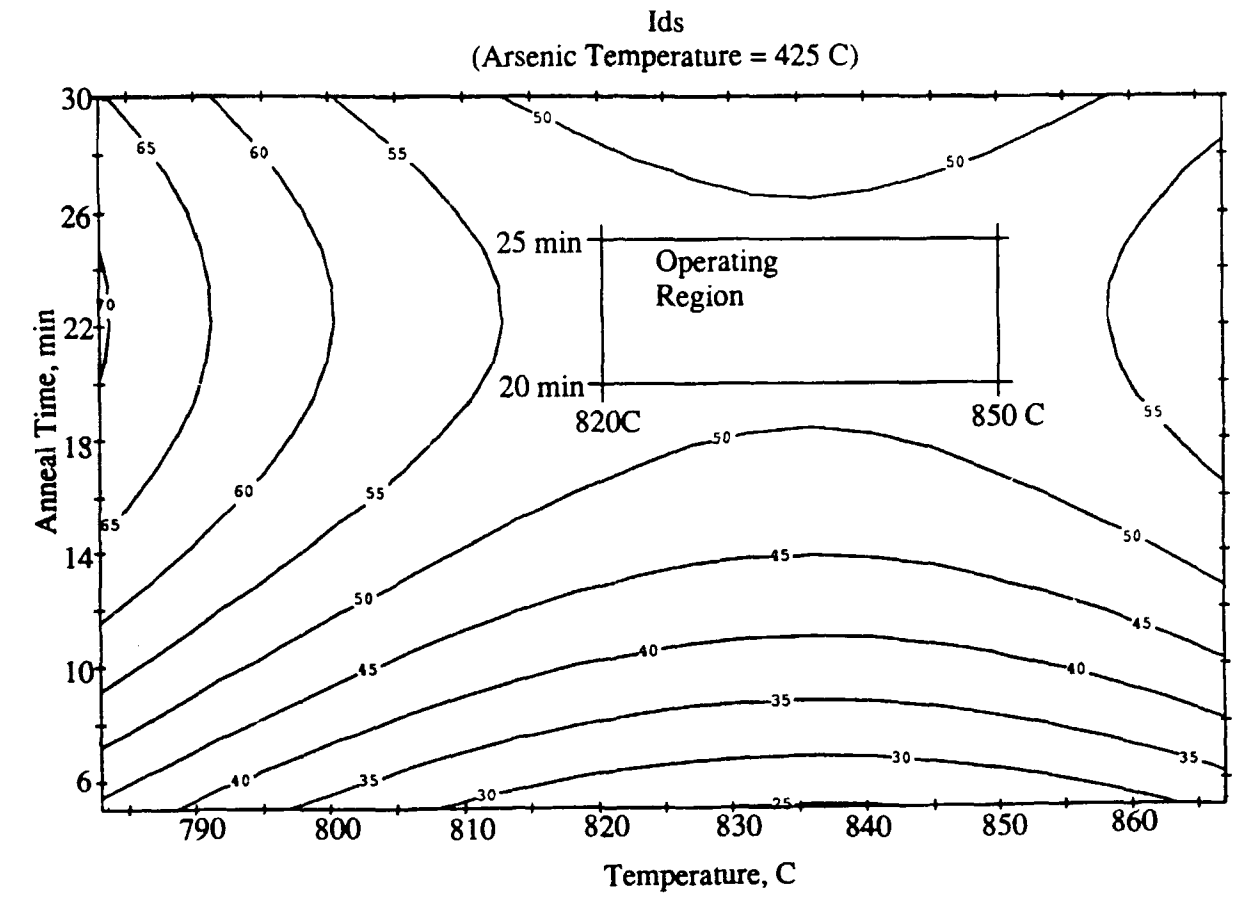
For our circuits, Ids is the most important parameter, so anneal time and temperature are set to minimize variations in Ids. We set the arsenic temperature by using the contour plot for gm, as shown in Figure 12 (bottom). The optimum arsenic temperature is 422°C, and gm will be constant within ±5% if the arsenic temperature can be held between 415 and 429°C, and anneal time can be held between (the already chosen) 20 and 25 minutes.

Not surprisingly, there are some situations where these choices of temperatures and time still leave some sensitivity to accidental variations in anneal parameters. Figure 13 shows a contour plot for Ids as it relates to anneal time and arsenic temperature. Within the range of data available, there is no flat region; but the chosen operating region is the best one available. Within the region already described, Ids will be constant within ±7%.

Experiment 3

The purpose of the third experiment was to validate the experimental model developed in the previous study and determine the sensitivity of the device characteristics to the anneal process in a more localized region. This experiment, which used the design described in the second study, also required 14 treatment combinations and six centerpoint replications. Table 15 contains the experimental treatment conditions. Here the intent was to cover many points within a small operating region.

As it turned out, run-to-run variation from MBE or from other wafer fab processes now dominate the experiment. We deliberately made small excursions around an operating point where the major device parameters are insensitive to annealing conditions. Table 16 shows that the correlation coefficients for these major device parameters (Ids, gm, Vi50 and V_{diode}) are lower for the third experiment than for the second experiment. This suggests that we can't improve our model by using data from Experiment 3. To do so, we would have to first replicate this experiment many times in order to average out the effects of the other random variation.


Ids
(Arsenic Temperature = 425 C)
Anneal Time, min
Temperature, C
25 min
20 min
Operating
Region
820C
850 C
30
26
22
18
14
10
6
790
800
810
820
830
840
850
860

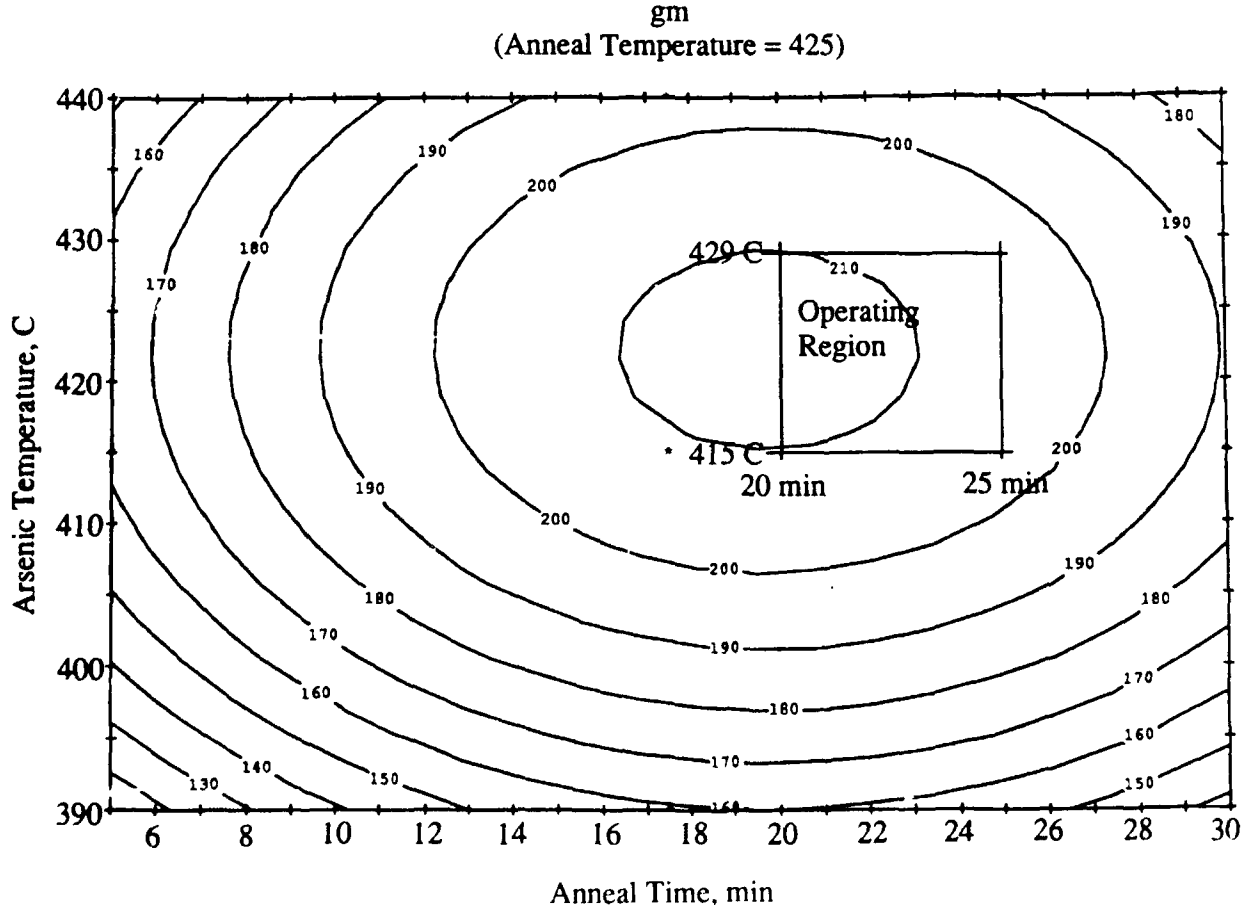
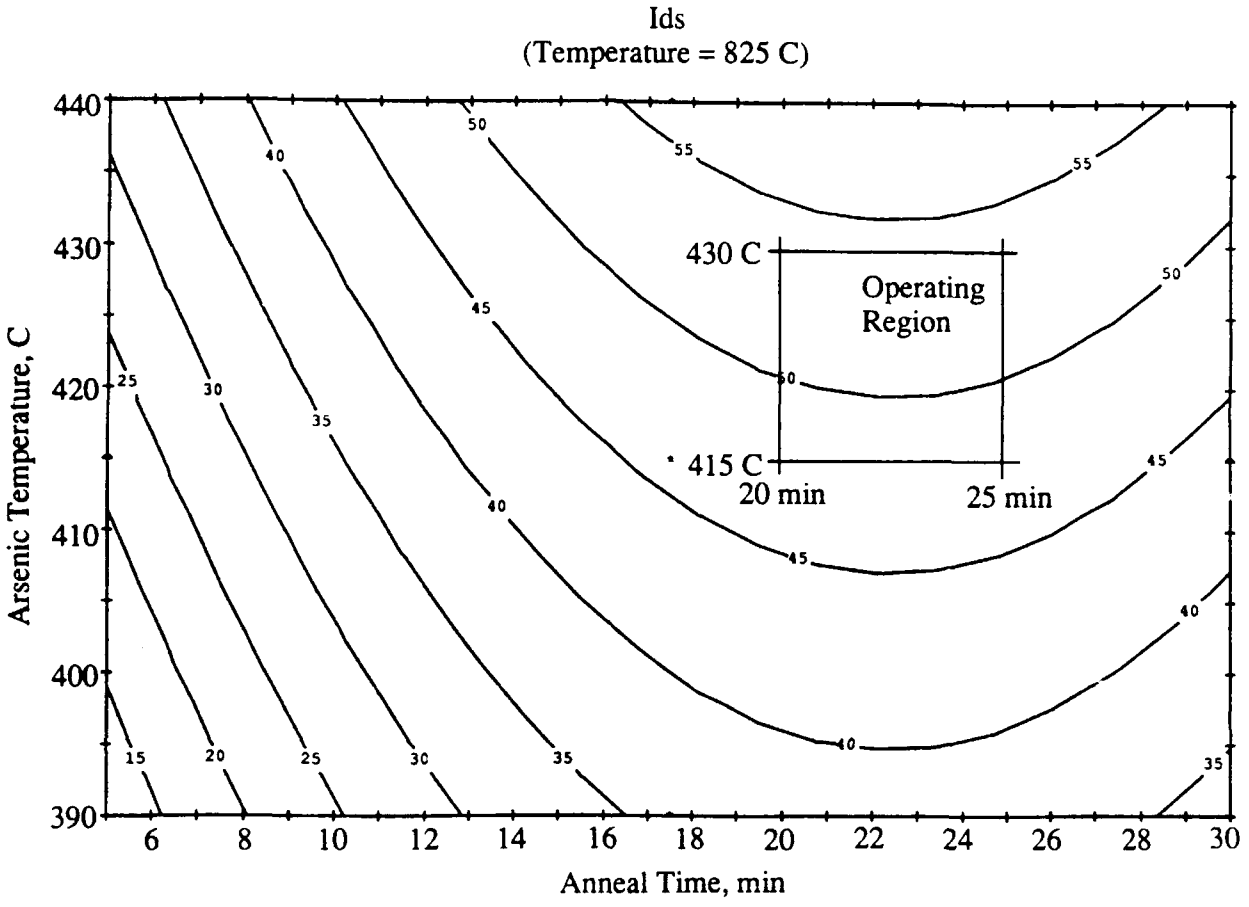

gm
(Anneal Temperature = 425)
Arsenic Temperature, C
Anneal Time, min
429 C
415 C
20 min
25 min
Operating
Region
440
430
420
410
400
390
6
8
10
12
14
16
18
20
22
24
26
28
30

Figure 12.



Contour Plot relating to Ids to Arsenic Temperature and Anneal Time

Figure 13.

TABLE 15 — Experiment 3 Treatment Conditions

Treatment Condition	Temperature (°C)	Time (min)	Arsenic Temperature (°C)
1	835	22.5	405
2	815	22.5	420
3	823	27.0	411
4	823	18.0	429
5	835	15	420
6	847	18.0	411
7	847	27.0	429
8	847	18.0	429
9	835	22.5	435
10	835	30.0	420
11	823	27.0	429
12	823	18.0	411
13	847	27.0	411
14	855	22.5	420
Centerpoint	835	22.5	420

TABLE 16 — Furnace Anneal Results for Experiment 3

Response	Correlation Coefficients	
Ids	0.57	Drain Current with Vgs=0.5V
Variance of Ids	0.76	
Ig	0.43	Gate Current with Vgs=2.5, Vds=0
Variance of Ig	0.56	
R_{out}	0.54	Output resistance with Vgs=0.5V
Variance of R_{out}	<0.10	
gm	0.55	gm at Vgs=0.5V
Variance of gm	0.38	
R_{N+}	0.80	Sheet resistance of N+ layer
Variance of R_{N+}	0.59	
R_N	0.59	Sheet resistance of N layer
Variance of R_N	0.90	
Vi50	0.57	Vgs for drain current=50 mA/mm
Variance of Vi50	0.70	
V_{diode}	0.55	Vgs at Igs=10μA/μm, Vds=0
Variance of V_{diode}	<0.10	

To relate device characteristics to furnace variables and to The accuracy of the model from Experiment 2 was gauged by comparing actual and predicted Ids values for an 835°C temperature, 420°C As temperature and 22.5 min. anneal. The average Ids value of 44.9 (±12)

mA/mm, calculated from a data set of 50 wafers, is positioned within the 95% (36 to 63 mA/mm) confidence interval predicted by the model. The actual wafer-to-wafer Ids variation of 12 mA/mm is only 3 mA/mm different from the 9 mA/mm value predicted from the model.

APPENDIX A

ADVANCED TECHNOLOGY

FINAL REPORT

TABLE OF CONTENTS

APPENDIX A
ADVANCED TECHNOLOGY FINAL REPORT

LIST OF FIGURES

1. INTRODUCTION (A. G. Baca, S. F. Nygren)

Under our contract for a Gallium Arsenide Pilot Line for High Performance Components (F29601-87-C-0202), DARPA asked us to "investigate (the) manufacturing feasibility of technology that is capable of achieving higher performance (at least a factor of two increase in speed or an order of magnitude in power) for the selected circuits ... picked for the main program." We chose to seek a factor of two increase in speed through two changes: 1) decreasing interconnect design rules to 1.5 μm lines and spaces (gate length is decreased from 1.0 μm to 0.75 μm), and 2) using an improved (faster) implementation of the SFFL logic gate. To provide a more robust wafer fabrication process for the decreased interconnect design rules, we developed an aluminum metallization process to replace the existing gold-based Baseline Technology.

As this report describes in detail, we believe we accomplished the goals of this program. By demonstrating 400 MHz operation with 20 gate delays, we achieved a factor of two increase in speed. Simultaneously, by examining yield data from process testers and actual circuits, we believe this Advanced Technology will have 30% of the manufacturing yield of the Baseline Process, thereby meeting the goals for manufacturing feasibility.

We developed our Advanced Process in two parallel paths. On one path, we developed a process for aluminum interconnect metallization. In comparison to our standard liftoff-patterned evaporated TiPtAu interconnects, we believe subtractively-patterned sputtered aluminum will provide better step coverage and superior metal definition, especially for the reduced line and space dimensions. As discussed in detail in Section 2, some key developments used in our aluminum process include a barrier to isolate aluminum from the gold-based ohmic contacts, thereby preventing "purple plague," and a dielectric planarization process to eliminate shorts. We processed both gold-interconnect wafers and aluminum-interconnect wafers using 1.5 μm lines and spaces. The gold interconnect wafers had via, crossover and serpentine yields comparable to our standard 2.0 μm line and space metallization process. Process testers with aluminum interconnects gave somewhat lower yields, but the planarization process had not been fully implemented when the evaluation was done.

On the parallel path, we confirmed that the Advanced Process would achieve the electrical performance goals (400 MHz for 20 gate delays, or 125 ps/gate). First, using ring oscillators, we demonstrated performance up to 926 MHz with 20 gate delays. Second, we fabricated 8x8 multiplier circuits with a total of 889 gates. Half the functional devices had gate delays equal to or shorter than 125 ps. Third, we examined the intrawafer and wafer-to-wafer variations in FET threshold using the Advanced Technology. These variations are two to three times as large as standard product from the same era. While we could expect to reduce variation somewhat as we refine our Advanced Technology, we believe further process development will be necessary to eliminate all the excess variation. All of these electrical tests were done with gold interconnects before the aluminum process development was complete.

Since our goal was to investigate manufacturing feasibility, we limited our work to developing a 1.5 μm aluminum interconnect process, measuring performance of circuits fabricated with 1.5 μm design rules, and making an initial characterization of reliability and radiation hardness. Overall, we're very pleased with the outcome of this study: we successfully demonstrated a factor of two increase in circuit speed without increasing circuit power consumption, and we demonstrated a potential for very high wafer fab processing yields with aluminum metallization. We also found that our diffusion barrier adequately prevents "purple plague" and that total dose radiation

hardness is unchanged from the Baseline Technology.

If there were plans to place this Advanced Technology into production, we found two remaining problems that need to be solved. First, the present aluminum interconnects have an unacceptably short life due to electromigration failures. This can probably be improved by altering the metal deposition conditions. Second, the transient dose radiation hardness is inferior to the Baseline Technology. This may be due to the smaller dimensions of the Advanced Technology and may be inherent to the process.

The remainder of this report describes the details of the development and characterization of this Advanced Technology in three sections:

- Process Technology
- Test Circuits
- Reliability and Radiation Testing

2. PROCESSING TECHNOLOGY

2.1 Aluminum Interconnects (R. J. Shul, A. G. Baca, R. M. Havrilla, S. E. Lengle)

The aluminum interconnect metallization process requires applying WSi as a barrier between the gold-based ohmic contacts and the aluminum interconnects, sputter depositing aluminum, patterning it into 1.5 μm lines and spaces, using sidewalls to eliminate aluminum stringers, and planarizing the structure to eliminate shorts due to aluminum left in troughs. We favor sputter-deposited aluminum over our standard evaporated TiPtAu interconnects because it provides better step coverage over vias. In addition, the subtractive patterning used with aluminum gives superior metal definition and fewer shorts compared to liftoff of TiPtAu interconnects.

Deposition

Aluminum is deposited in an MRC 943 sputtering system from a composite target consisting of 0.5% Cu and 99.5% Al. The Cu is included to minimize electromigration. The thickness is chosen to match the sheet resistance of the baseline technology TiPtAu interconnects; we use 8000Å for aluminum bottom metal and 10,600Å for aluminum top metal.

Lithography

Due to the reflective nature of aluminum, conventional fine line lithography is not possible. To reduce reflection by about 50%, we use a WSi_x coating over the aluminum. Then we can routinely pattern 1.5 μm lines and spaces with a 5x stepper.

Reactive Ion Etching

Etch

Aluminum is patterned in a BCl_3/Cl_2 plasma operating in a reactive ion etch mode. Including BCl_3 in the etch chemistry helps expose aluminum to the plasma by removing oxide and minimizes the incubation time for etching. The reactive ion etch mode promotes a more physical, anistropic etch with vertical Al sidewalls; without the reactive ion etch mode, there would be severe undercutting.

Corrosion

Post etch corrosion is one of the major considerations in the subtractive patterning of Al (see Figure 1). The presence of residual Cl catalyzes the corrosion of Al in the presence of moisture. This can be overcome by introducing an in-situ fluorine passivation. The patterned Al sample is exposed to an SF_6 plasma, which exchanges F with residual Cl, forming involatile products and eliminating corrosion. The use of BCl_3 also helps eliminate water from the chamber, which is held at approximately 58°C to reduce water absorption.

After the wafers are removed from the chamber, they are rinsed in water to remove any remaining Cl. Use of a water rinse often results in a phenomenon referred to as "mouse bites . Mouse bites are localized regions of missing metal usually seen at the edges of lines or pads (see Figure 2). This can result in open interconnect lines or areas of excessively high resistance which might result in premature failures. Altering the pH of the deionized water slightly eliminates mouse bites.

Corrosion of Al lines over GaAs. The Al was not exposed to a passivation step following the BCl_3/Cl_2 etch.

Figure 1.

Mouse bites are missing pieces of metal which are often observed at the edge of features. This is observed following the water rinse to remove residual Cl.

Figure 2.

Barrier

The use of Al interconnects our technology introduces a complication due to the interaction of Al interconnects and Au from the ohmic contacts. Interdiffusion of Al and Au can lead to the formation of high resistivity intermetallics often referred to as "purple plague." We developed a conductive diffusion barrier to separate Au from Al because these high resistivity intermetallics can cause premature circuit failures.

The barrier is a multi-layer WSi_x structure (see Figure 3). Following the evaporation of ohmic metal, 1000Å of WSi_x is sputter deposited over the substrate and defined by the ohmic liftoff process. The ohmic metal feature is therefore encapsulated by WSi_x. The sputter deposition of WSi_x decreases the reliability of the liftoff process, increasing the likelihood of burrs. Burrs have been observed for the 1.5μ design rules, but we saw no evidence of shorts.

To further prevent interdiffusion of Au and Al, an additional layer of WSi_x, 2000Å, is sputter-deposited in-situ, just prior to Al deposition. This layer of WSi_x is patterned with the same lithography as the Al interconnect lines and is etched in-situ following the Al etch. Thus the WSi_x barrier is patterned by the Al lines. Step coverage is still an issue with this technique, and we may require a plug process.

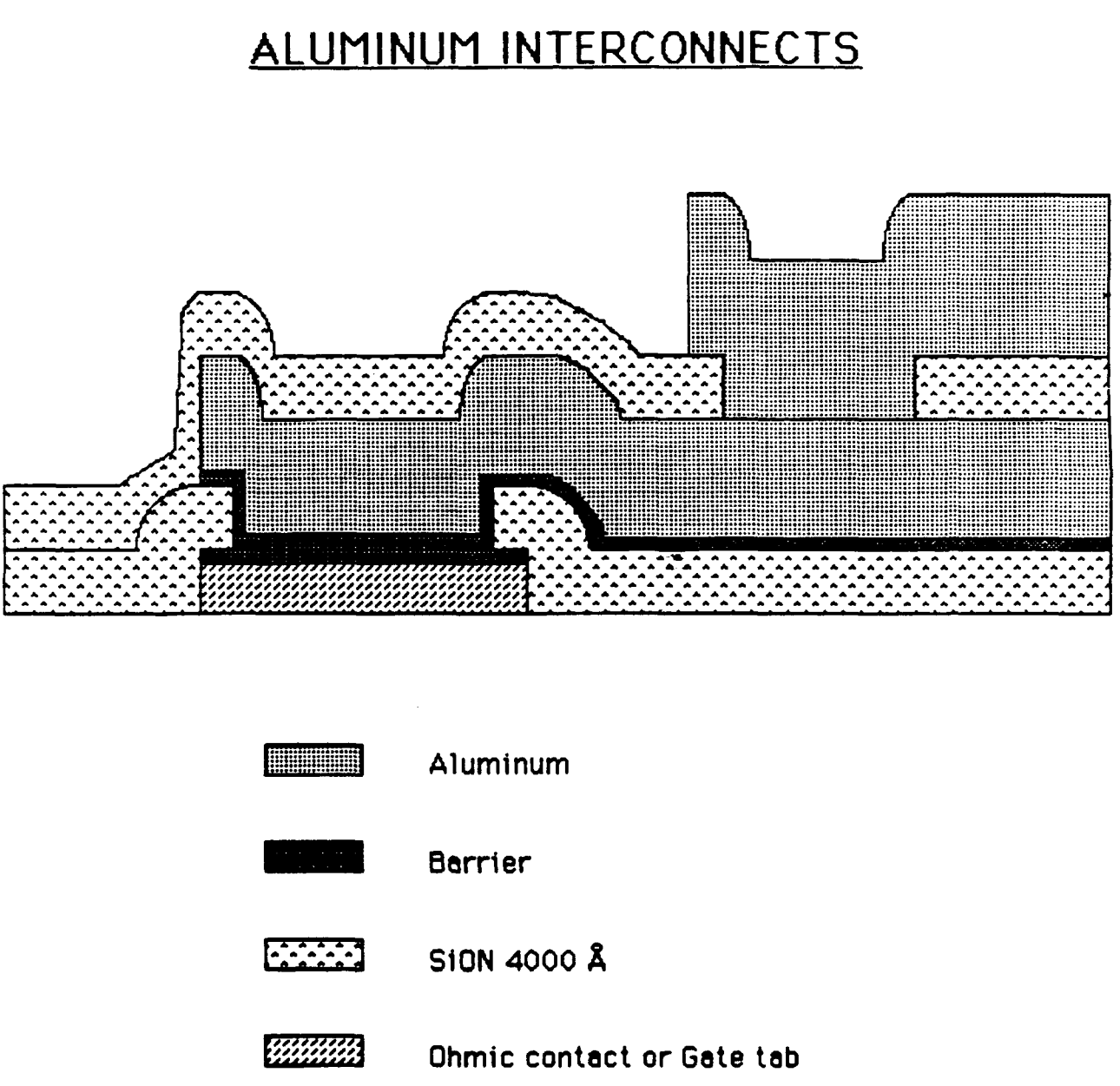
First Level Aluminum Interconnects

A multi-step, in-situ etch is incorporated to remove the thin anti-reflective WSi_x layer (SF_6 etchant), pattern Al (BCl_3/Cl_2 etchant), passivate residual Cl and pattern the WSi_x barrier layer (SF_6/O_2 etchant), and initiate photoresist removal (O_2). The wafers are then removed from the chamber and rinsed in deionized water.

Preliminary etch experiments for Al interconnects were on PT-Y samples. (See Section 2.2 for an expanded description of PT-Y.) Al etching over ohmic metal pads (AuGeNi) reproducibly yields anisotropic lines and shows no sign of corrosion (see Figure 4). However, shorts were observed in via chain test patterns of Al interconnects etched over gate metal (WSi_x). Figure 5 shows filaments or stringers of Al remaining in the via chain patterns where dielectric (4000Å) covers gate metal. Significant overetching did not remove the Al stringers. With the aid of SEM photographs, we saw cusping of dielectric over gate metal (see Figure 6).

Gate metal is patterned by reactive ion etching, creating a sidewall profile which is concave (see Figure 7). The dielectric covers the features conformally and cusps around the gate. Cusping is not observed over ohmic, which is patterned with a liftoff process and has a smooth rounded profile which the dielectric covers smoothly. Since the FET characteristics are very sensitive to the gate process, steps were taken to change the dielectric coverage without changing the gate profile.

We developed a sidewall process, based on a thick dielectric deposition and etchback. Deposition of 6000Å of SiON followed by reactive ion etching in CF_4 resulted in a smooth profile of dielectric over the gate with no cusping (see Figure 8). Since the sidewall etch is endpointed over GaAs and requires an overetch for uniformity, damage to the substrate was observed. Preliminary experiments show that annealing at 390°C for 30 seconds removes the majority of damage observed in threshold voltage and current. Al is then deposited and etched with no sign of stringers or shorts.

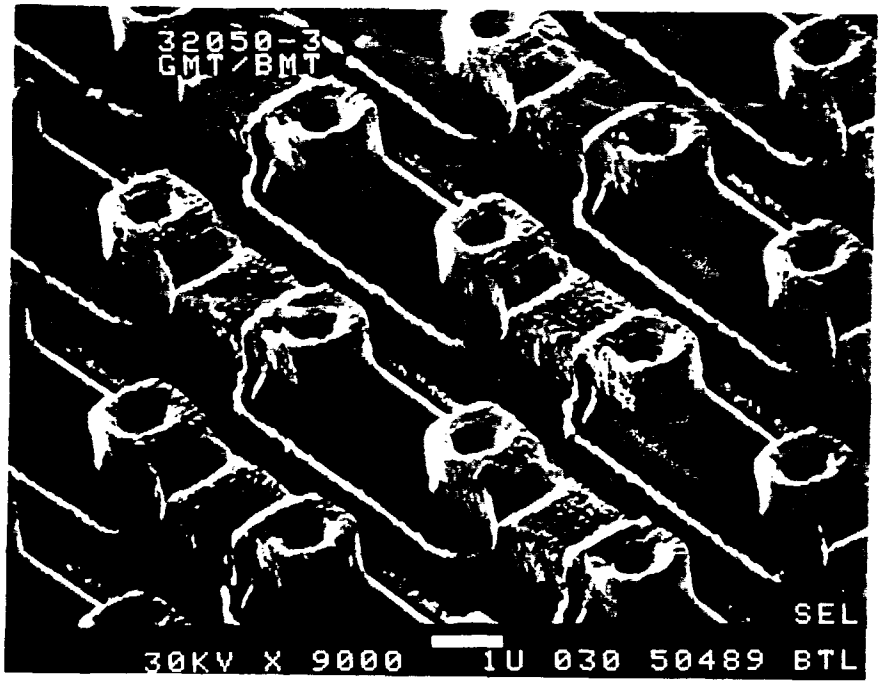


Schematic diagram of Al interconnect with the WSi_x diffusion barrier.

Figure 3.

SEM of patterned Al lines over ohmic metal features.
The ohmic metal is covered with 4000Å of SiON.

Figure 4.



SEM of patterned Al lines over gate metal.
Notice the remaining Al (stringers) around the SiON
which covers the gate feature.

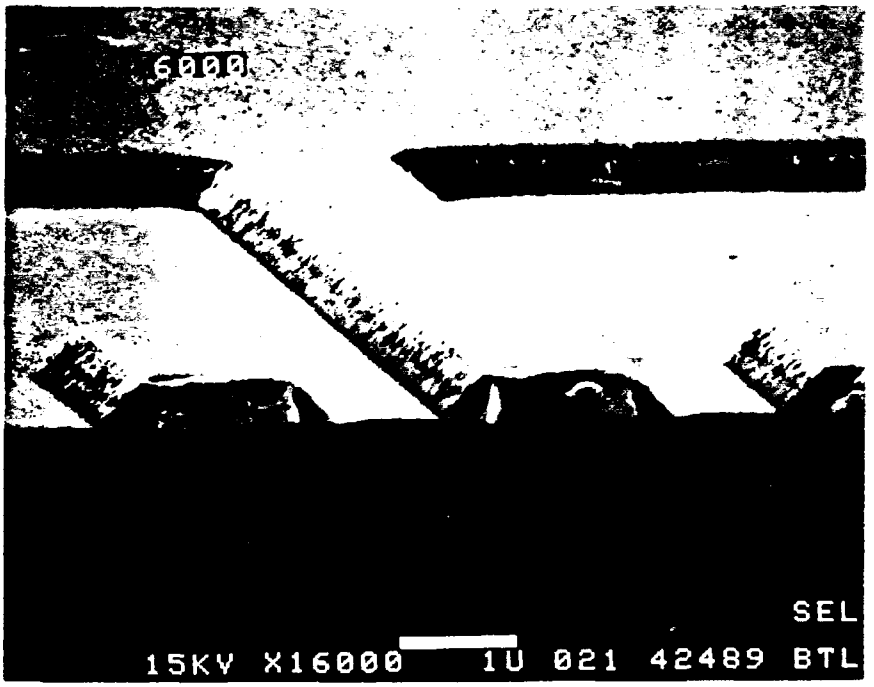
Figure 5.

SEM which shows the dielectric (SiON) coverage over ohmic and gate metal. The ohmic is patterned with a liftoff process and has a rounded profile which the SiON covers smoothly. The gate is patterned with a subtractive etch process and is concave creating a cusp in the dielectric profile resulting in Al stringers.

Figure 6.

SEM showing the WSi_x gate profile.

Figure 7.



The profile of the gate is changed with the integration of a sidewall to prevent cusping.

Figure 8.

Second Level Aluminum

Design rules specify that second level interconnect is only allowed to contact first level interconnect, so that a barrier for Au/Al diffusion is not required. Following via 2 formation, second level Al is deposited and etched. Preliminary work showed Al filaments over first level Al due to the vertical profile of the Al lines. To circumvent this problem the sidewall process was also introduced following first level Al. Successful integration of this step has been achieved with no observation of Al stringers or shorts.

An aspect ratio of approximately 1:1 (width to depth of the trough) following second level dielectric and sidewall deposition is observed prior to second level Al metallization. Complete removal of Al in the trough is necessary to prevent premature failures due to shorts. The process described so far shows mixed results as observed by SEM pictures and comb/serpentine electrical testers, with some samples showing complete Al removal, and others showing severe shorting. These results indicate the necessity for a more robust process utilizing planarization.

Planarization

The process of choice for aluminum metallization includes fully planarized interlevel dielectric. Following first level metallization (ohmic and gate), a 10,000Å thick layer of SiON is deposited. The SiON contours to the features of the ohmic and gate metals leaving a non-planar surface. Photoresist (10,250Å) is then spun-on to achieve a planar profile (see Figure 9). A_oCF_4/O_2 etch is used to etch the photoresist and the SiON at comparable rates (2300 to 2400Å/min.). This leaves a planar profile of SiON (4000Å) over the ohmic and gate metal. This process works over 1.0μ gate and ohmic features (see Figure 10) and can be incorporated for multi-level metal schemes.

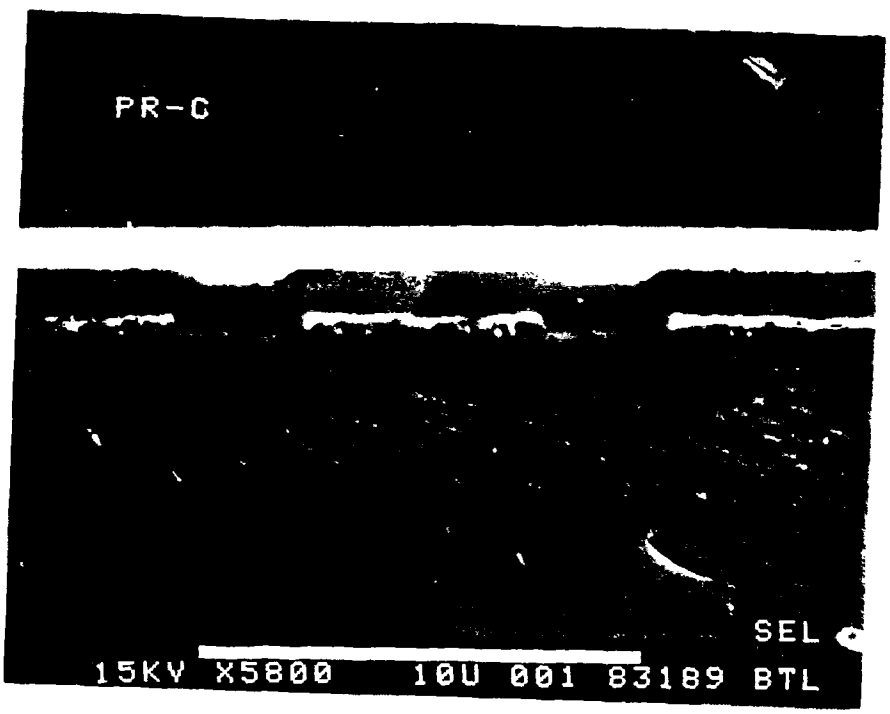
Future Work

At this stage, we have demonstrated all the steps of aluminum processing needed for the Advanced Technology. Since our goal was to investigate feasibility, there is no need to proceed further. If this process were placed into production, two further steps would be needed. First, the interlevel dielectric planarization process must be integrated with the rest of the process. Second, we saw intermittent burrs in the liftoff of the thin WSi used as a barrier between gold and aluminum. We need to develop a via plug process that will function as a barrier to diffusion and purple plague, eliminate liftoff of sputtered metal, and improve topography.

2.2 Process Tester Characterization (A. G. Baca, D. D. Manchon, R. J. Shul)

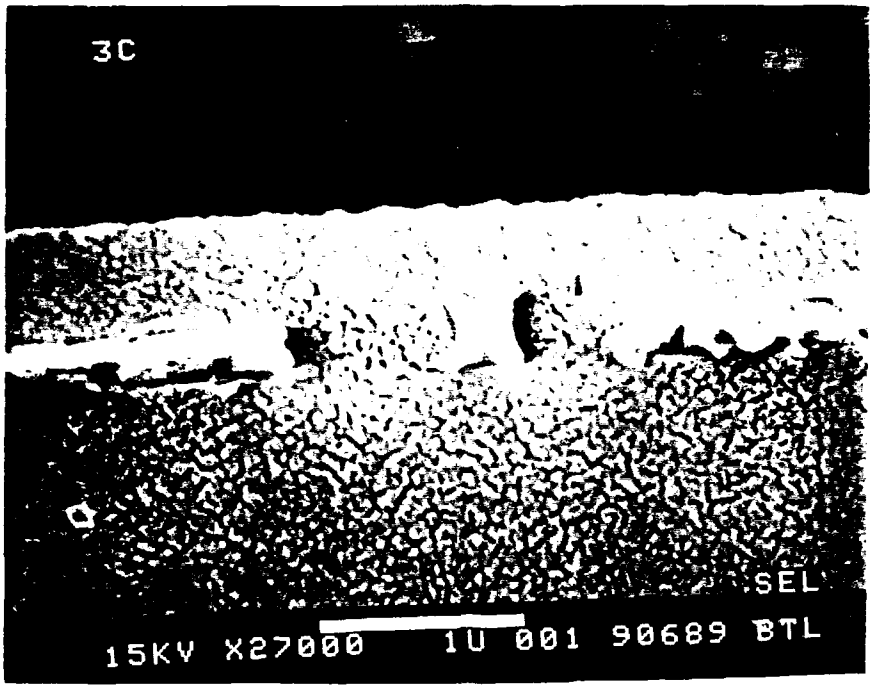
Compared to our Baseline Technology, the Advanced Technology process consists of HFETs and interconnect metallization shrunk by 25% (except for vias which are shrunk from 1.5 μm to 1.0 μm). We use the same MBE substrate as in the Baseline Technology. Process characterization falls into two categories: assessing expected yield based on our ability to fabricate the smaller features, and assessing our ability to maintain parametric control with the short channel HFET. We characterized the Advanced Technology using both gold-based and aluminum interconnects to separately show the effects of shrinking the size and of changing to aluminum.

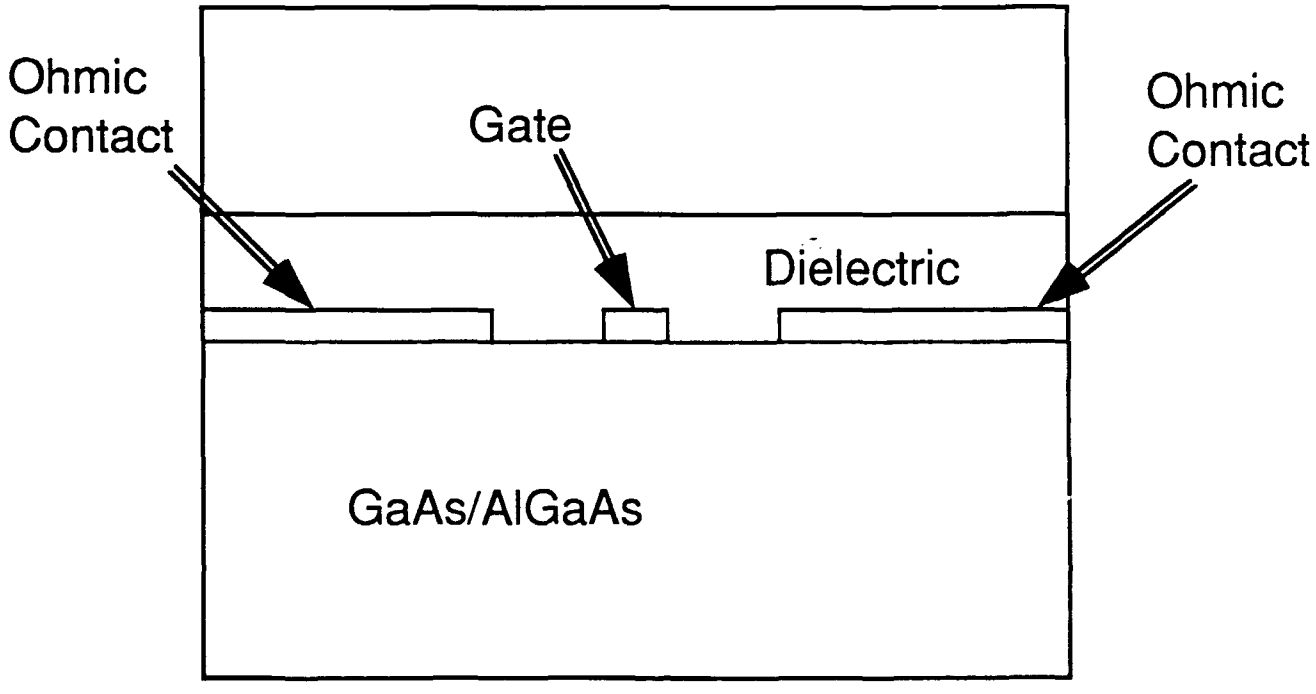
Threshold voltage control was monitored for 21 wafers from five lots with 0.75 μm nominal gates (actual gate length measured 0.65 μm compared to 0.90 μm for the Baseline Technology). Figures 11 and 12 show inter- and intra-wafer variation. The variability is 2-3x greater than the



A nearly planar profile is achieved by thick deposition of dielectric followed by spinning on a thick layer of photoresist.

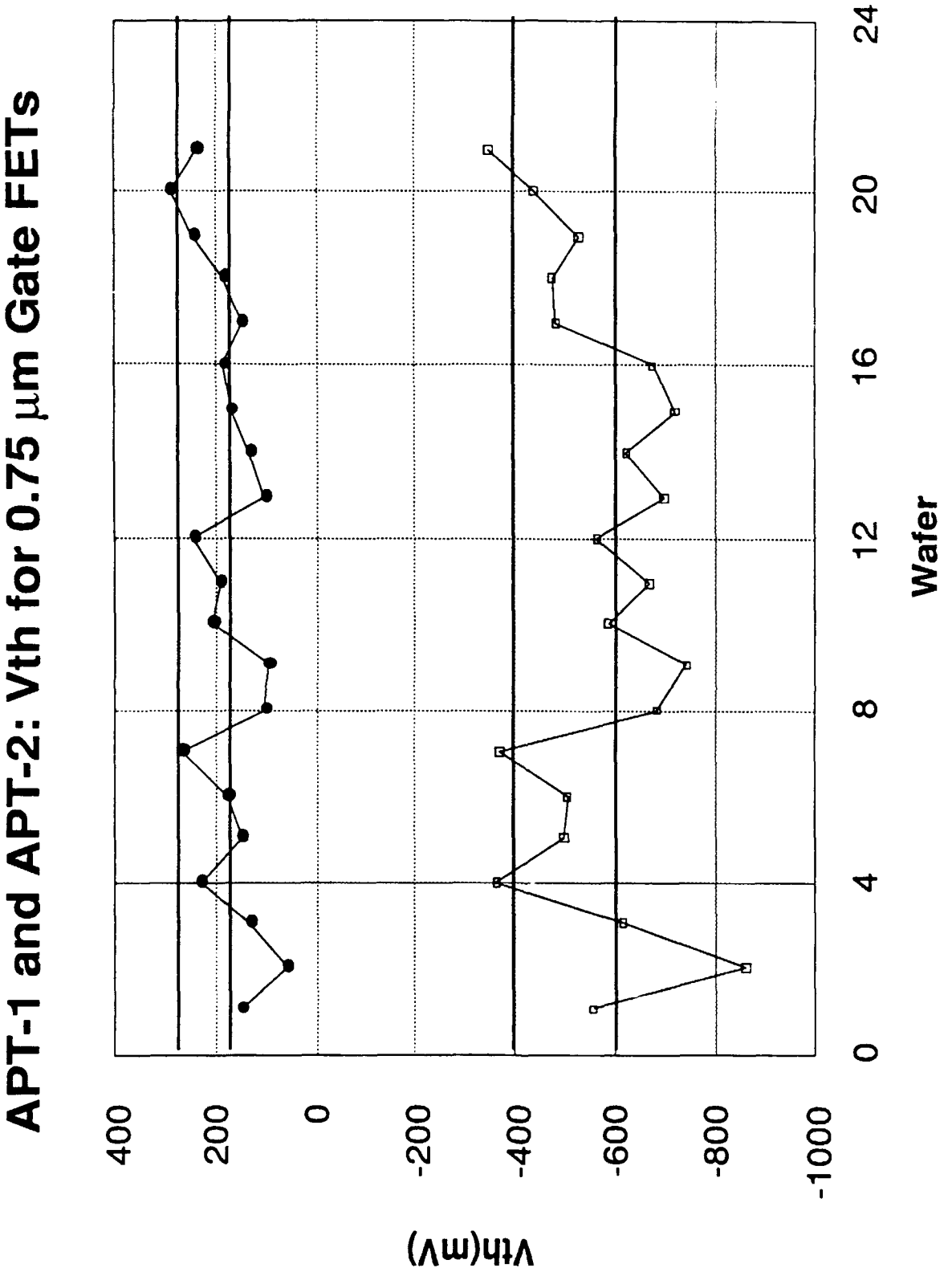
Figure 9.





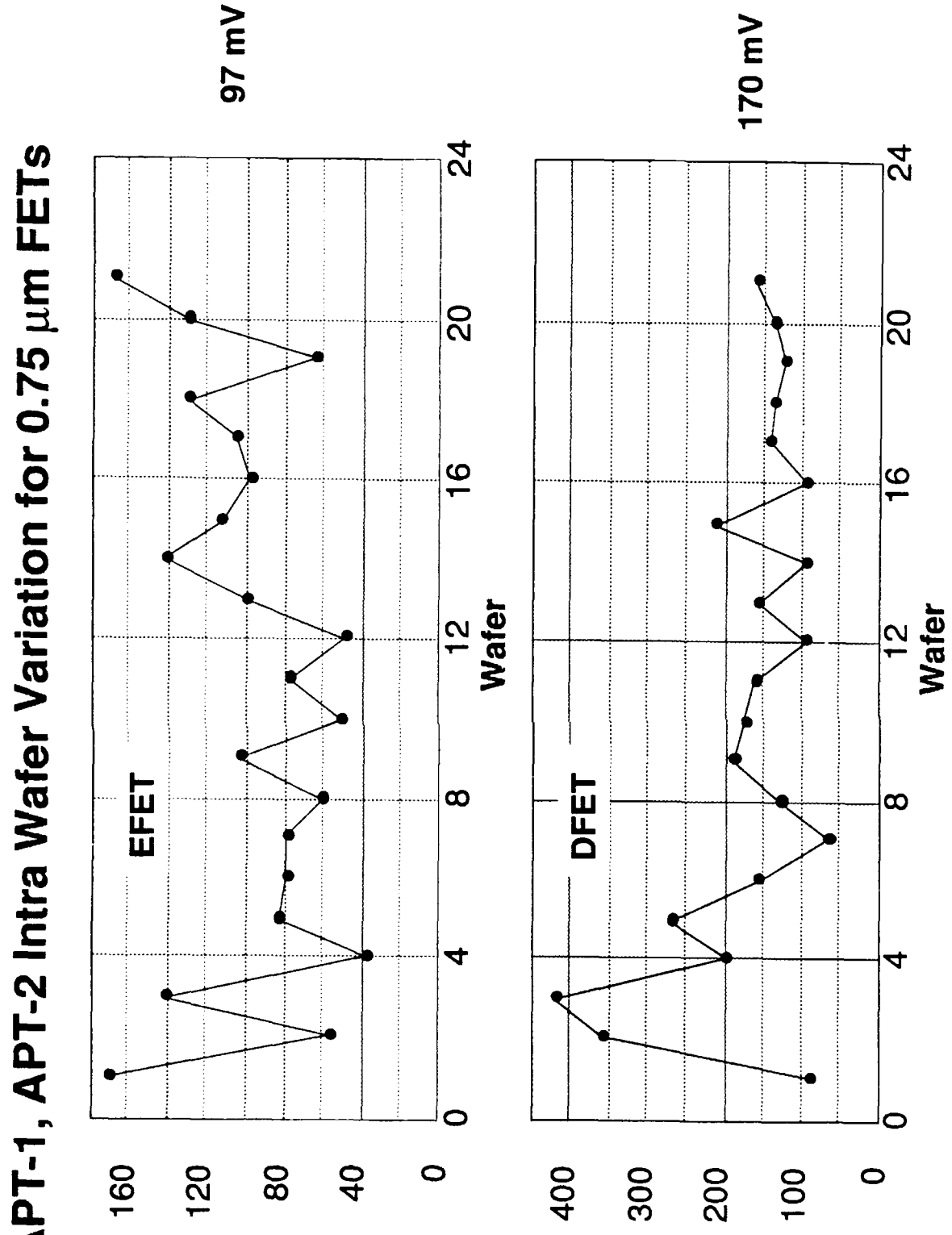
A planar profile can be obtained if the etch rate of the photoresist and dielectric are comparable.

Figure 10.



Wafer-to-wafer threshold variations for EFETs and DFETs in the Advanced Technology.

Figure 11.



Intrawafer standard deviations of thresholds for EFETs and DFETs in the Advanced Technology.

Figure 12.

Baseline Technology of the same era. We expect that some of this variation can be reduced through using process Failure Mode Analysis (FMA) to uncover and eliminate sources of variation, as has been done in the Baseline Technology. However, short channel effects are responsible for a major part of this variation, and it is expected that a process enhancement such a lightly-doped drain structure will be required to further reduce the variation.

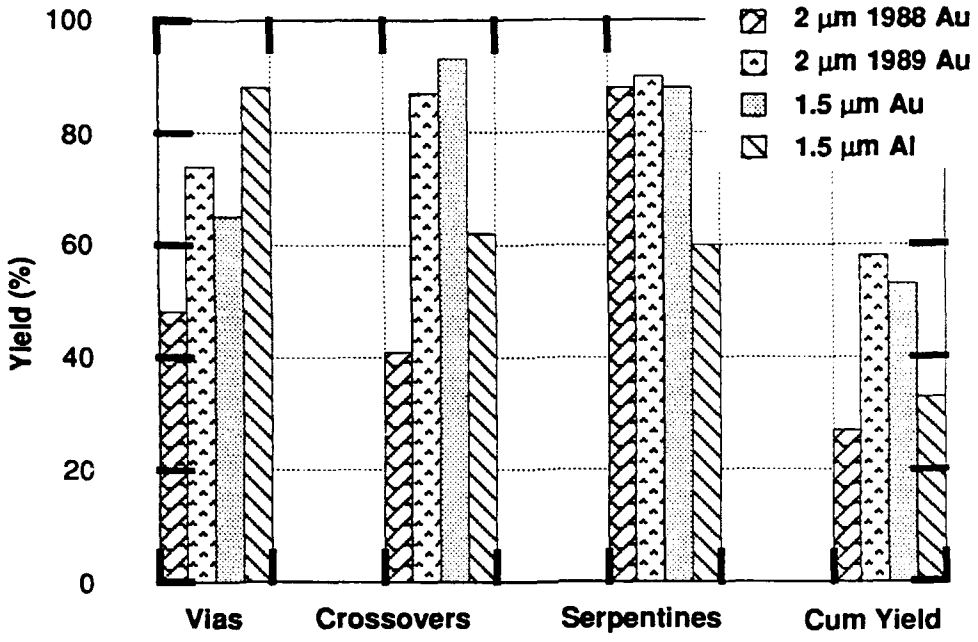
A three level metal tester, one FET level and two interconnect levels, was designed and used to characterize the Advanced Technology metallizations with 1.5 μm design rules. This new tester, called PT-Y, was used to compare the Al process with the Au-based liftoff process, as well as to compare 2.0 and 1.5 μm design rules. Metal shorts within a process level are tested by means of serpentine/comb testers (serpentines interleaved with combs) of up to 19 cm of adjacent metal. Dielectric integrity and shorts between metal levels are tested by means of combs and/or serpentine testers on different levels with up to 250,000 crossovers in 1.5 μm design rules and up to 181,500 crossovers in 2.0 μm design rules. Vias are tested by serpentines connecting different metal levels with up to 250,000 vias in 1.5 μm design rules and up to 181,500 vias in 2.0 μm design rules. A via tester is labeled "good" when the entire via serpentine is continuous with the proper resistance. A serpentine/comb metal crossover tester is "good" when the entire site shows no shorts between metals tested. Data are presented as actual or extrapolated to 250,000 for vias and crossovers.

A summary of the results is shown in Figure 13. The 1988 Au data comes from PT-X in early 1988. The Au data for 1989 comes from 20 wafers processed in four PT-Y lots. The figure shows that the baseline 2.0 μm technology showed major improvement from the early 1988 results. Compared to the 1989 2 μm Au, the 1.5 μm Au yielded somewhat lower for vias and serpentines and slightly higher for crossovers. For 1.5 μm gold, both the area and feature size are smaller. The smaller area tends to increase the yield, and the smaller feature size decreases the fatal defect size and thus lowers the yield. The net effect is a slightly lower yield for the 1.5 μm design rules. No lots had catastrophic failures with 1.5 μm design rules using liftoff processing; however, this technology is expected to be much more difficult to control in production. Compared to 1989 2 μm Au, the cum yield (the product of the via, crossover, and serpentine yield) is 10% less for 1.5 μm design rules using Au.

The aluminum data comes from ten wafers from two PT-Y lots. The Al process with 1.5 μm design rules yielded greater for the via process because of the better metal coverage into the via. However the crossover and serpentine yields are lower. As noted in the previous section, incomplete removal of Al in the high aspect ratio troughs is responsible for the lower serpentine yields. This problem will be eliminated by planarization. The extremely vertical Al profile and resultant sharp metal edges put more stress on the dielectric and are probably responsible for the lower crossover yields; planarization should improve this yield, also. The cum yield for the advanced Al process is 38% less than for the advanced Au process. However, the higher via yields demonstrate the promise of an Al process.

We conclude that very acceptable metallization yields have been achieved with 1.5 μm design rules. We believe that the process of choice is a fully planarized Al process using the methods described in the previous section.

Interconnect Comparisons



	Baseline		Advanced	
	Au PTX	Au PTY	Au	Al
Via Yield*	48%	74%	65%	88%
Crossover Yield*	41%	87%	93%	62%
Serpentine Yield**	88%	90%	88%	60%
Cumulative Yield	17%	58%	53%	33%
Via Do (cm-2)	17.8	7.2	20.1	5.3
Crossover Do	22	3.5	2.7	21
Serpentine Do	8.2	8.6	18.8	75

* Yield for 250,000 via (crossover) testers

** Yield for 19 cm of metal - metal runners at minimum space

Comparison of interconnect yields in the Advanced Technology

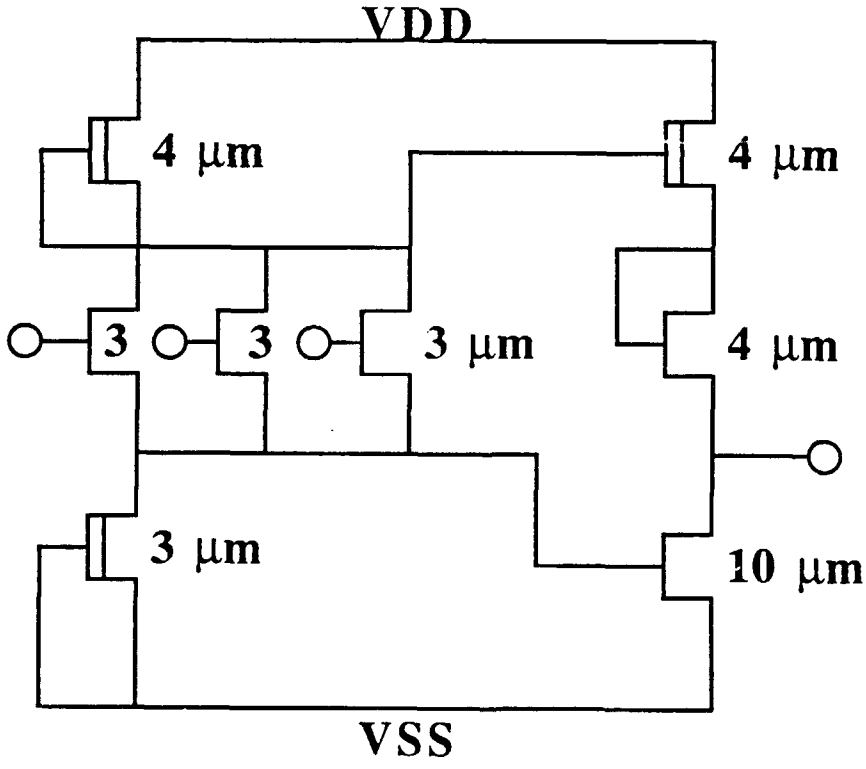
Figure 13.

3. TEST CIRCUITS

Two mask sets were designed to test the performance of the Advanced Technology: APT-1 tests characteristics of FETs and the logic family. APT-2 tests multiplier performance. Both mask sets could be fabricated with either gold or aluminum interconnect metallization. Since development of the aluminum process proceeded in parallel with circuit testing, we often used gold interconnects to test concepts before the aluminum process was ready.

3.1 Ring Oscillator (P. J. Robertson, A. I. Faris, A. G. Baca)

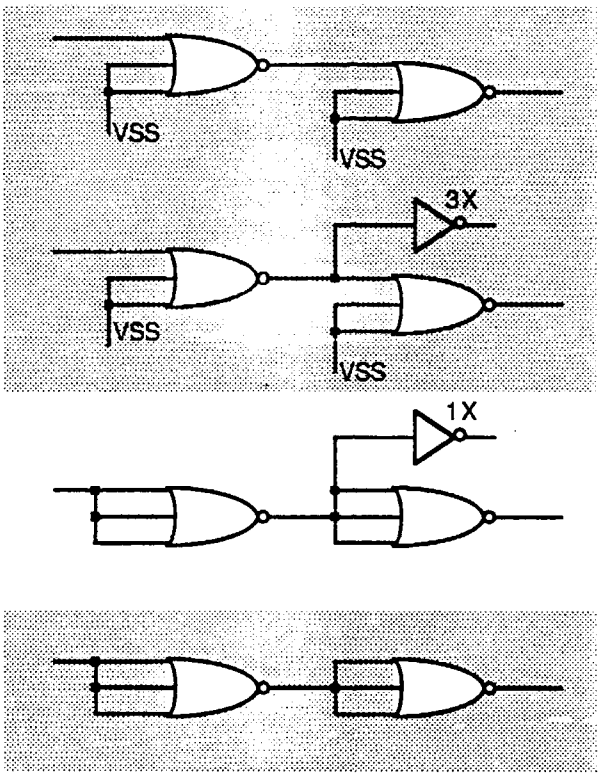
The APT-1 mask set consisted of 31-stage ring oscillators with logic elements that used the Low power Source Follower FET Logic (L-SFFL) logic family. A schematic of a typical 3-input nor gate is shown in Figure 14. The logic stages used in the ring oscillators were of four basic types varying in the number of fanins and fanouts as shown in Figure 15. We used gold interconnect metallization to fabricate wafers using the APT-1 mask set. (At this early stage of development, aluminum wasn't ready.)



L-SFFL 3-Input NOR Gate

Figure 14.

The L-SFFL logic gates were designed and simulated using the SargicS.11 models to operate with a E/D current ratio of 0.71. The actual as-processed wafers had E/D current ratios that were as small as 0.29. This resulted from negative threshold shifts in the transistor characteristics brought about by the shorter gate lengths[1] used for the Advanced Process.



Circuit variations for APT-1 Ring Oscillators.
Fanin = 3 and Fanout = 4 was chosen for comparison since FET characteristics were shifted off-target by the short gates.

Figure 15.

Table 1 shows Process Control Module (PCM) data for the FETs on APT-1, where EFET currents are measured at V_{gs} = 0.5 V and V_{ds} = 2.0 V, and DFET currents are measured with V_{gs} = 0.0 V and V_{ds} = 2.0 V.

1. The standard Sargic process has a nominal gate length of 1.0 μm. The Advanced Process used nominal gate lengths of 0.75 μm.

TABLE 1 — FET Current Characteristics for PCM Measurements vs. the Nominal SargicS.11 Model Values. The SargicS.11 models were used to design the APT-1 circuits.

	EFET (V_{gs} = 0.5 V)	DFET (V_{gs} = 0.0 V)	E/D Current Ratio
SargicS.11	50 mA/mm	70 mA/mm	0.71
Lot 31710	50 mA/mm	170 mA/mm	0.29
Lot 31920	75 mA/mm	125 mA/mm	0.60

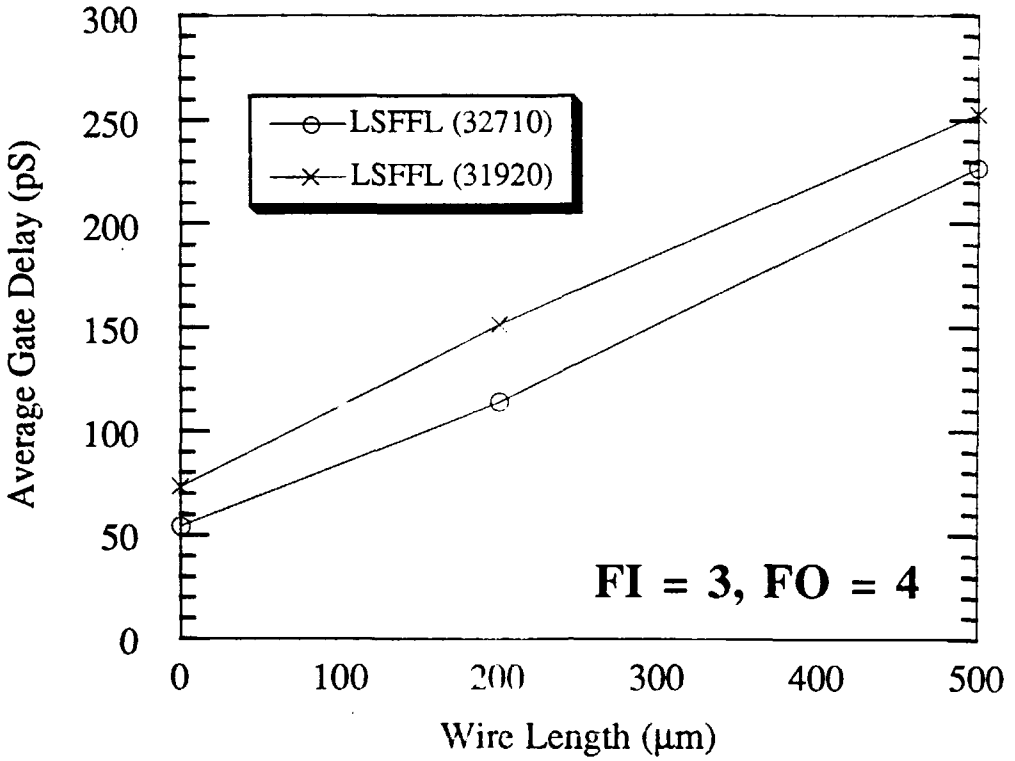
Since the current ratios did not match the design specifications, it was necessary to drive all three inputs of a 3-input NOR gate in order to get proper logic levels. Thus, we evaluated the data from ring oscillators with fanin = 3 and fanout = 4. Comparisons were made between three wire load lengths (0, 200 and 500 μm). The power supply voltage was 2.0 volts.

Measurements from Lots 31710 and 31920 are summarized in Table 2. The speed of operation of circuits in lot 31710 would be slightly less than 1GHz with 20 gate delays.[2] These results indicate that the Advanced Technology circuits surpass the Advanced Technology objective of 400 MHz operation with 20 gate delays. The power*delay product for the Advanced Technology circuits is excellent. Lot 31710 has a power*delay product of 49 fJ and lot 31920 had 42 fJ. The data in Table 2 is shown in graphical form in Figure 16.

TABLE 2 — Summary of the Average Gate Delay Measurements for APT-1.

	Average Gate Delay	
Length	Lot 31710	Lot 31920
0 μm	54 pS	73 pS
200 μm	114 pS	151 pS
500 μm	227 pS	253 pS

2. Maximum frequency with 20 gate delays: Lot 31710 = 926 MHz; Lot 31920 = 685 MHz.



Plot of Average Gate Delay Versus Wire Length

Figure 16.

3.2 8 x 8 Multiplier (R. J. Niescier)

To demonstrate the capability of the Advanced Technology in a meaningful circuit, we chose a standard cell design that was previously fabricated in the Baseline Technology 2.0 μm AT&T HFET process. The two's complement 8x8 integer multiplier from PT-2L was chosen because it contained eleven unique standard cells which were grouped into only five macrocells. Because it was a standard cell design, only the macrocells had to be redesigned and our standard cell router would place the power busing and interconnect. The placement of the macrocells was already determined by the previous design. We could therefore investigate the Advanced Technology performance with a minimal investment in design and layout resources.

The function of this multiplier is to accept two eight bit two's complement integer numbers and produce a sixteen bit two's complement result. The partial product reduction is accomplished with a simple carry-save array and the final summation is performed by a carry propagate adder. The gate count in the critical path is 46 and the total gate count of one multiplier is 889.

The ease with which this circuit could be redone allowed the addition of two more modifications to the multiplier. Two more primary sites, in addition to the control site and the standard Advanced Technology site, were designed as experiments for side-gating and scaling. The side-gating site was identical to the Advanced Technology site except that the FETs were packed as closely as possible with some even sharing the same isolation area. The scaling site was identical to the control site except that it was linearly shrunk from the 2.0 μm rules to the advanced 1.5 μm

rules. This experiment, if successful, would allow the linear shrink of the baseline circuits with only a minimum NRE cost, instead of a large redesign and layout cost. All these designs were placed on the APT-2 mask set, where each reticle field contained four sites:

- Site 1: A direct copy of the PT-2L Multiplier using 2.0 μm design rules.
- Site 2: A linear shrink of all components of the PT-2L multiplier to test scaling effects. In Site 2, a feature is 75% of the size in Site 1.
- Site 3: Like Site 4 (the standard Advanced Technology site), except that the FETs were packed as closely as possible, sometimes sharing the same isolation area.
- Site 4: The standard Advanced Technology design using 1.5 μm lines and spaces. In this case, to try to avoid scaling problems, the minimum gate width was kept the same as the Baseline Technology.

We demonstrated circuit performance in APT-2 with gold metallization and 0.75 μm gates (except for Site 1, which uses 1.0 μm gates). Aluminum metallization was also attempted, but the lots were fabricated before the barrier metal process was fully developed, and they all failed due to gold/aluminum interactions. Because 1.0 μm gates give different FET thresholds than 0.75 μm gates, Site 1 failed to function.

For the required 400 MHz operation with 15 - 20 gate delays, we require operation at 125 ps/gate. Of 312 multipliers tested, 56 functioned at some value of V_{DD}, I/O voltage, and speed; 26 worked at 125 ps/gate or faster. Four circuits repeatably ran at 90 ps/gate at close to the 2.0V target supply voltage. For the functioning sites, circuit performance is given in Table 3.

TABLE 3 — APT-2 YIELDS

Site	Functional	Speed	I/O	Average Current
2	12%	6%	0%	0.561 A
3	24%	11%	8%	0.447 A
4	17%	8%	4%	0.482 A

Functional: passed test vectors at some I/O, speed, and V_{DD}
Speed. faster than 125 ps/gate at some I/O and V_{DD}
I/O: functioned at V_{DD}=2.0 V, V_{ih}<1.0 V, V_{il}>0.3 V, for any speed

These tested devices all came from two wafers, and there was noticeable variation in performance for different areas in the wafers. For example, chips from the tops of the wafers drew twice the current of chips from the bottom. Also, while all input buffers in these three sites were the same, there was considerable I/O performance variation. This makes it hard to draw specific conclusions, but some general trends are clear. First, Site 2 (the linear, or "dumb" shrink) did not perform well. Its characteristics are similar to those seen previously when small FETs show threshold shifts compared to larger EFETs. Because of the dumb shrink, Site 2 contains EFETs with small widths (i.e., 3-5 μm). Second, while Site 3 shows higher yields than Site 4, Site 4 seems to produce more robust circuits. That is, while none of the tested circuits on APT-2 simultaneously meet speed, power supply, and I/O specifications, Site 4 has the most sites with better performance. These are limited data, but we believe that appropriately separated FETs with proper isolation (i.e., Site 4) lead to the best performance.

Extrapolation of Circuit Yield

The objective of the Advanced Technology is to achieve both suitable performance and a predicted 3% DC functional yield. As described above, we developed this process along parallel paths. Along one path, we developed an aluminum metallization process. Simultaneously, along the other path, we used gold interconnects (with 1.5 μm lines and spaces) to demonstrate circuit performance.

For vias, serpentines, and crossovers, we showed above that 1.5 μm gold interconnects have a 10% lower yield than 2.0 μm gold interconnects (see Section 2.2). In addition to that, there are two ways to look at the circuit yield.

- Table 3 shows a 17% functional yield for Site 4. This compares with a 27% yield achieved in prior data with the PT-2L version of the same circuit. This is a 37% yield reduction for the Advanced Technology.
- Alternatively, we can compare PCM yields for the two technologies in comparable time periods. Then the Baseline Technology has a 28% PCM yield, while the Advanced Technology has a 6.4% PCM yield. This is a 77% yield reduction for the Advanced Technology.

Multiplying the interconnect yield times the circuit yield, we find that the Advanced Technology has a 21 - 57% yield compared to the Baseline Technology. That is, when the Baseline Technology achieves a 10% yield, the Advanced Technology is expected to have a 2.1 - 5.7% yield. This compares to the 3% goal.

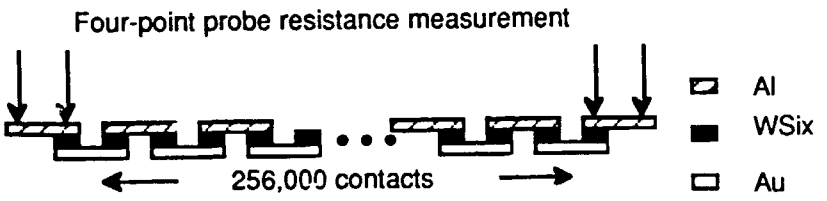
We showed in Section 2.2 that the via, serpentine, and crossover yield is 38% lower for 1.5 μm aluminum than for 1.5 μm gold. However, that yield was obtained with an aluminum process that omitted the desired planarization step. When planarization is integrated into the aluminum metal process, we expected a yield comparable to or better than gold.

4. RELIABILITY AND RADIATION TESTING

4.1 Diffusion Barrier Thermal Aging (P. F. Thompson)

As part of the aluminum metallization process, we introduced a diffusion barrier to prevent gold-aluminum interactions at the ohmic contacts (see Section 2.1). We used thermal aging test wafers to get a preliminary indication of the diffusion barrier performance.

Wafers in the thermal aging study used test structures containing a series connection of ohmic metal (Au) - metal 1 (Al) interfaces (with the intervening WSi_x diffusion barrier) (Figure 17). The test structures are called via chains. Two wafers were aged; one passivated with 4000Å SiON dielectric over the metal, and one with no dielectric. There were 15 test structures measured on the non-passivated wafer, and 24 test structures measured on the passivated wafer. Aging lasted 1000 hours at 200°C. Four point resistance measurements were taken at intervals during the aging process.



Via chain test structures

Figure 17.

After 1000 hours, there were no failed (open) via chains or increases in via chain resistance. In fact, resistance decreased during aging. The decrease closely fit an exponential decay to a constant resistance, suggesting additional annealing of the metal structure. While no quantitative prediction of lifetimes was possible (or intended) from this preliminary study, some indication of the diffusion barrier effectiveness is possible. Since this study consisted of non-biased thermal aging, gold-aluminum interdiffusion (as opposed to aluminum electromigration) would be the likely failure mechanism. Peck & Zierdt (Proc. IEEE, Feb., 1974) presented Al-Au bonding failure data in a review article showing activation energy data and relating temperature to time to fail. From their data, 0.1% failures would be expected after 1000 hours at 200°C. One failure in a via chain would be 3.9×10^{-4}% failures. Even if the first failure in the test patterns occurred at 1000 hours, the cumulative percent failures is 256 times less for the test pattern, based on a single via chain, than for direct gold-aluminum contact. Although we can't say the via lifetime will in fact be 256 times that of gold-aluminum bonds, the results indicate a significant beneficial effect from the WSi_x diffusion barrier.

4.2 Interconnect Reliability (P. F. Thompson)

Electromigration testing was performed on both gold and aluminum interconnects. The goal of the tests was to predict interconnect reliability for AT&T's metallization processes as of February, 1990. No prior electromigration tests had been performed on aluminum, and no recent tests had been performed on gold. The following sections describe the experimental plan, procedure and results, and data analysis.

Experimental Plan

Equation 1 describes metallization electromigration lifetime.

$$L_2=L_1\exp[E_a/R(1/T_1-1/T_2)]X(j_1/j_2)^n \quad (1)$$

where:

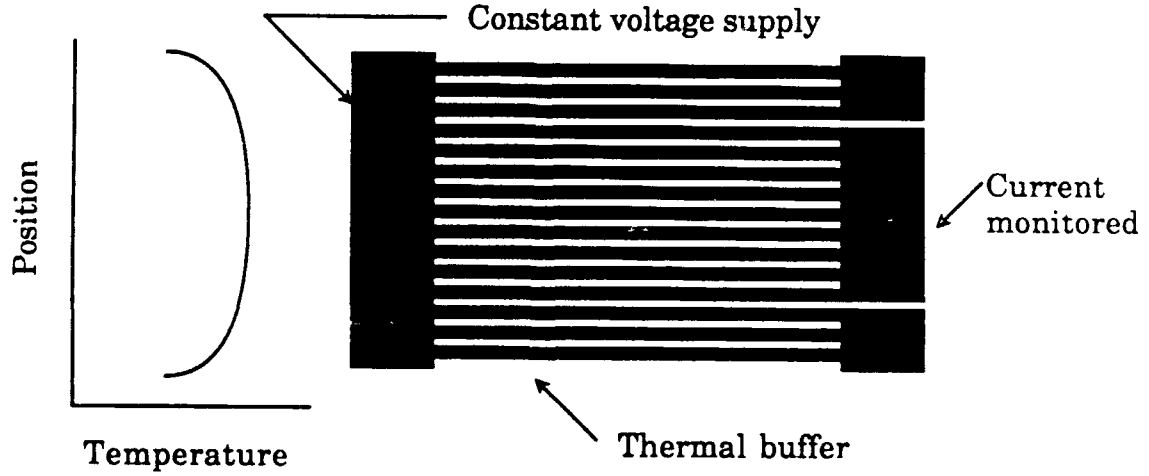
L_i=lifetime at condition i
T_i=temperature at condition i
j_i=current density at condition i
E_a=activation energy
n=current acceleration exponent

By aging test structures at multiple temperature and current density combinations as shown in Table 4, we expected to compute "best fit" values of E_a and n for each metallization (aluminum and gold). The test structure used three groups of parallel lines as shown schematically in Figure 18. The central group was bracketed by smaller side groups intended to serve as temperature buffers. We chose the current densities to span a wide range while minimizing joule heating. Then the temperature of the central group is essentially constant as indicated at the left side of Figure 18.

TABLE 4 — Test conditions for electromigration testing.

ALUMINUM			
T(°C)	$j(10^5 Acm^{-2})$		
	5.21	10.5	16.3
150°C	X		X
175°C		X	
200°C	X		X

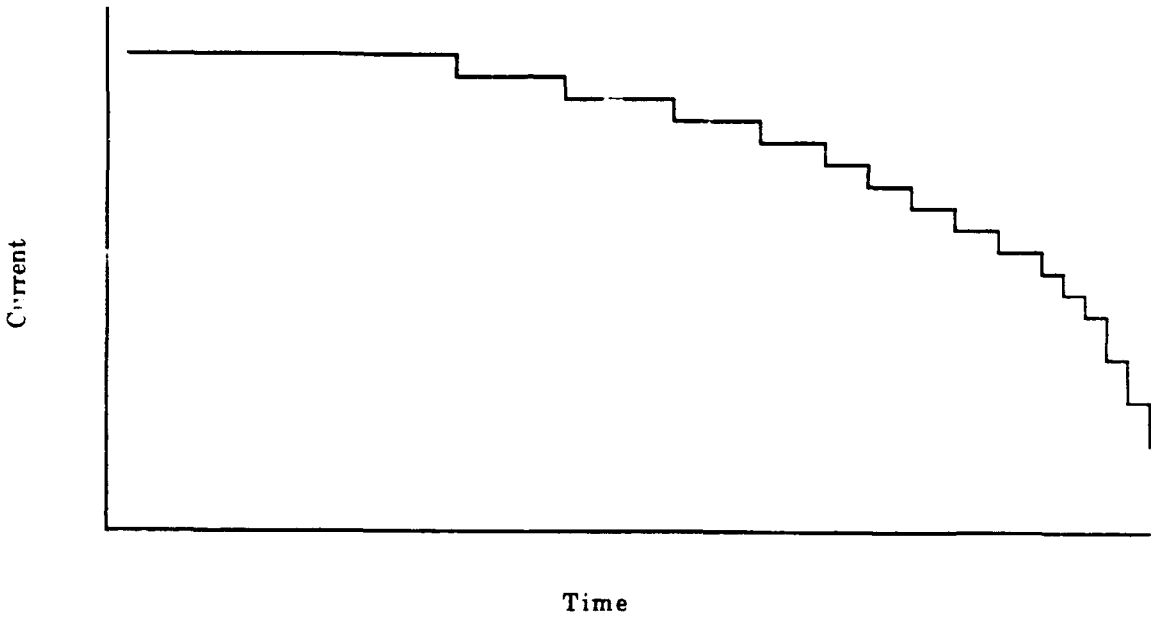
GOLD			
T(°C)	$j(10^5 Acm^{-2})$		
	3.92	10.0	15.7
150°C	X		X
175°C		X	
200°C	X		X



Parallel Line Test Structure

Figure 18.

These test structures were packaged and placed in ovens with automatic data acquisition. Data were recorded essentially continuously (one recording for each 1/100 of the time on test). Approximately 20 testers were used at each combination of temperature and current density. Voltage was maintained constant, and current was monitored. As indicated in Figure 19, failure of a conductor line results in a step decrease in current. We used about 50 lines per tester, so the data for each tester provides a failure time distribution.



Current vs. time curve for a parallel line test structure. Each step change indicates one or more stripe failures. The number of failures can be determined from the step height.

Figure 19.

Experimental Results

Unfortunately, we only obtained failure distributions in 2 of the 10 experimental cells. First, there were no gold failures within the duration of the experiment (2000-2300 hours). Second, a computer crash during the 50-100 hour interval destroyed all data in that interval and also destroyed the initial values of the 150°C aluminum cells. Consequently, median lifetimes were obtained for only aluminum aging at 175°C (10.5×10^5 Acm^{-2}) and 200°C (16.3×10^5 Acm^{-2}), as shown in Table 5.

TABLE 5 — Median lifetimes in hours at accelerated conditions.

ALUMINUM			
T(°C)	j(10^5 Acm^{-2})		
	5.21	10.5	16.3
150°C	(1)		(1)
175°C		91	
200°C	<100(1)		0.65

GOLD			
T(°C)	j(10^5 Acm^{-2})		
	3.92	10.0	15.7
150°C	>2295(2)		>2295(2)
175°C		>1950(2)	
200°C	>1950(2)		>1950(2)

1. Data lost in computer crash.
2. No failures.

Despite the experimental difficulties, this experiment clearly shows the status of the two metallizations: Gold from this vintage is consistent with expectations, where aluminum has noticeable short comings. By using information from the literature, we can compute various expected lifetimes based on the data we collected. For aluminum, we use E_a = 0.5 eV and n = 1.5; for gold we use 0.7 eV and 1.5. (These are the generally accepted values and/or the values in the center of the reported ranges.) Table 6 gives expected lifetimes for aluminum at 2.0 x 10^5 Acm^{-2} (the MILSTD 883C limit) and gold at 4.0 x 10^5 Acm^{-2} (AT&T's limit for GaAs interconnect). As indicted in the footnote to the table, the gold metallization actually has a longer life than given in the table, because (for the purpose of illustration) the table assumes gold failures at the end of the test duration even though there weren't actually any failures.

TABLE 6 — Lifetimes for different use conditions.

Use Temp (°C)	Aluminum (hours)	Minimum Gold (hours)*
100	15000	$1.5x10^6$
125	5600	$3.9x10^5$
150	2400	$1.2x10^5$

*Assumes median gold failure time is the test duration, although no failures had actually occurred at that point.

These relatively short lives for aluminum metallization are disappointing. Visual inspection of the aluminum metallization failures showed voids at random locations. There was no evidence of corrosion or failure at the bus locations, so all failures appear to be electromigration. Before this aluminum process could be used for production, we would require additional development to achieve acceptable reliability. For example, aluminum deposition conditions could be varied to alter the metallization grain size. Since other organizations successfully use aluminum metallization, this problem is clearly not insurmountable. However, since the requirement of this program was simply to demonstration feasibility, we have not undertaken further development at this time.

4.3 Radiation Testing (S. B. Witmer, M. Spector)

Total Dose

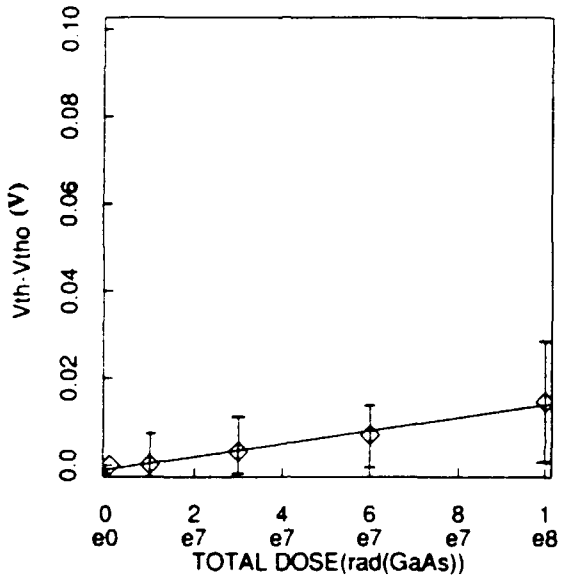
Total dose radiation testing was performed on (gold interconnect) Advanced Technology discrete FETs and ring oscillators. The devices were exposed to gamma radiation up to $1x10^8$rad(GaAs) from a Co^{60} source. The average change in threshold voltage (ΔV_{th}) after $1x10^8$rad(GaAs) was 18 mV and 22 mV in EFETs and DFETs, respectively (see Figure 20). In comparison, ΔV_{th} at 1 x 10^8 rad (GaAs) for the Baseline Technology was 20 mV and 40 mV. A 10% decrease in oscillation frequency in ring oscillators was also observed at $1x10^8$rad(GaAs) (see Figure 21). These results are comparable to the Baseline Technology total dose results.

Transient Ionizing Dose Testing

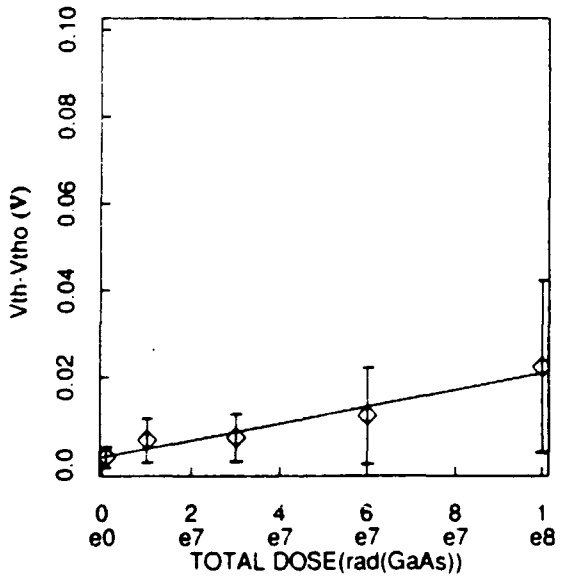
Transient ionizing dose testing was performed on (gold interconnect) Advanced Technology FETs and ring oscillators from two different lots. The results were lot dependent; but, in general, the radiation-induced drain current during the 30 ns radiation pulses was larger than in Baseline Technology FETs.

APT ring oscillators stopped oscillating at dose rates of approximately $5x10^8$rad(GaAs)/sec with recovery time in milliseconds. These results differ greatly from the Baseline Technology ring oscillators where oscillations stopped at approximately $5x10^9$rad(GaAs)/sec with prompt recovery times of less than 50 ns.

(A)



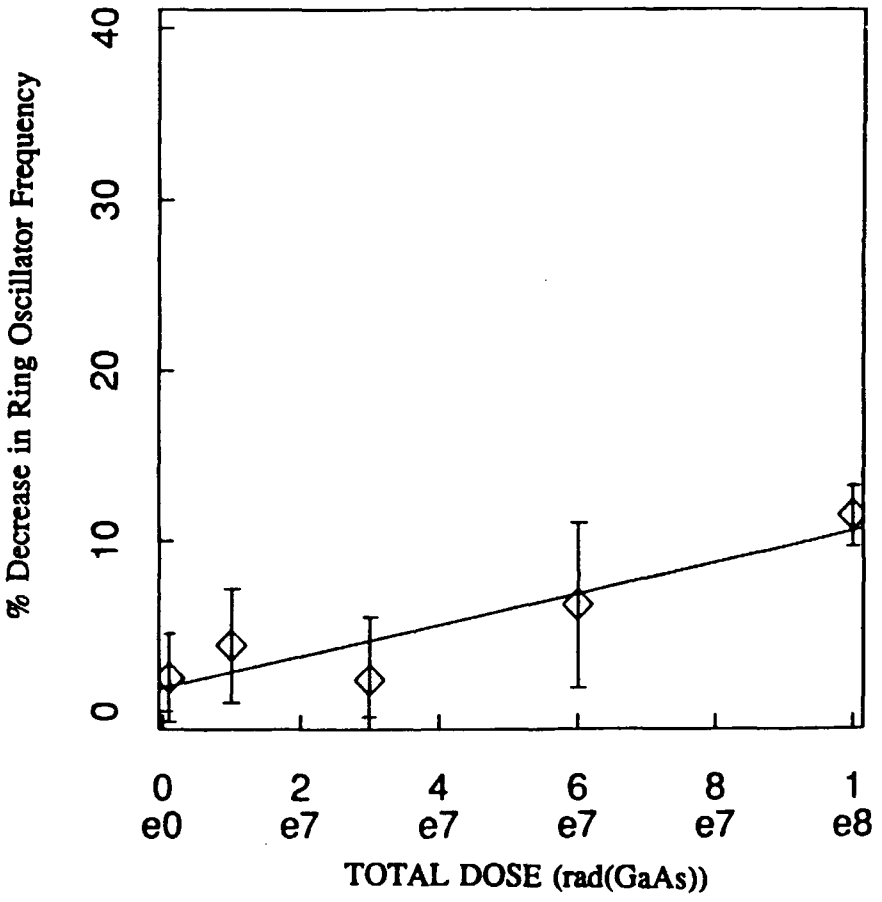
(B)



Change in threshold voltage versus total dose gamma radiation of advanced technology (APT) (A) EFETs and (B) DFETs.

Total dose effects in Advanced Technology HFETs (Gamma Radiation)

Figure 20.



Total Dose Irradiation of Advanced Technology Ring Oscillator

Figure 21.